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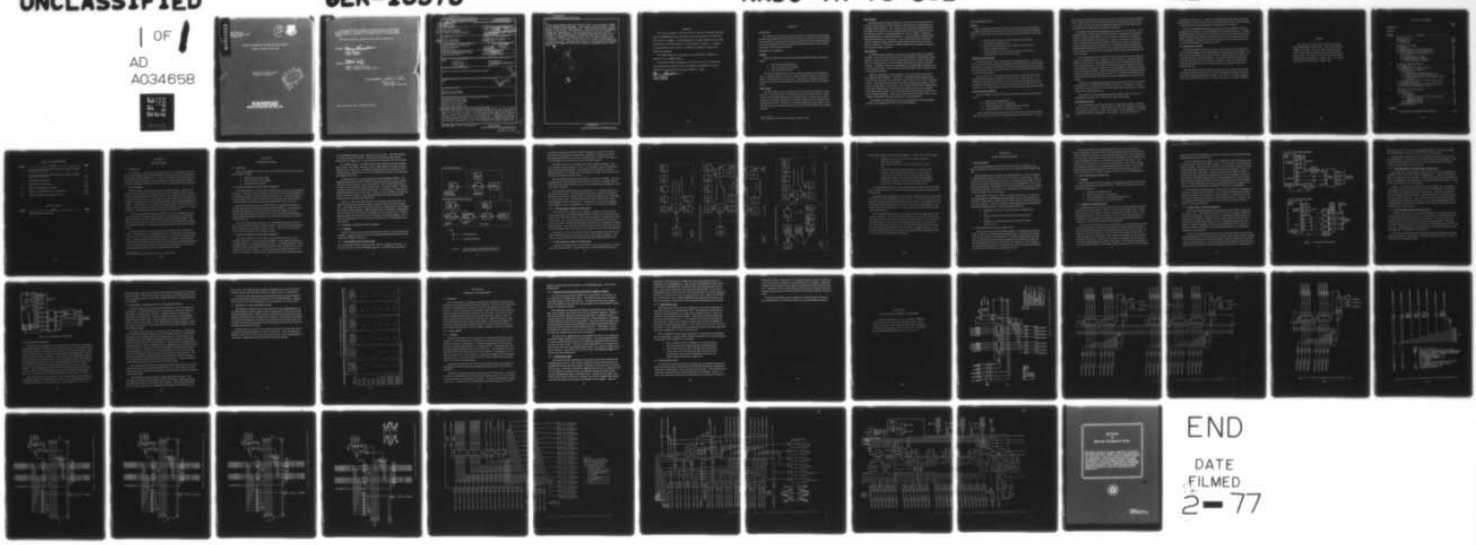

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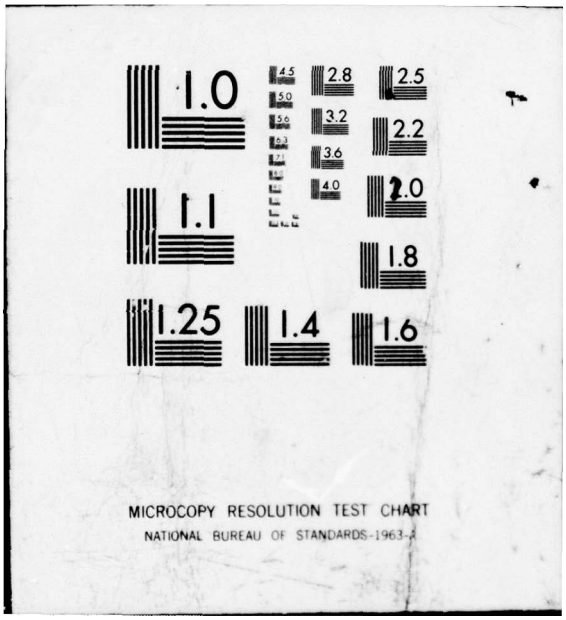
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Final Technical Report
November 1976

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ASSOCIATIVE PROCESSOR I/O DESIGN AND SPECIFICATION

Goodyear Aerospace Corporation

ROME AIR DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
GRIFFISS AIR FORCE BASE, NEW YORK 13441

This report has been reviewed by the RADC Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Detailed input/output (I/O) specifications were compiled for the three interface channels that currently exist in the STARAN associative processing computer at RADC: (1) buffered I/O (BIO), (2) direct memory access (DMA), and (3) external function (EXF). The availability and location of port connections for these channels are included within the I/O specifications. A comprehensive philosophy was developed that provides an interface between various external devices and the parallel input/output PIO unit. The recommended PIO expansion method uses

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a daisy-chain approach, where each external device is constrained to repeat all the signals of the PIO channel. The expansion method contains a control channel and four 256-bit-wide data ports. These data ports connect external devices to the PIO unit. The associative arrays also connect to the PIO unit through four existing ports. Since the associative array ports contain intermediate buffer registers, the recommended expansion data ports are not buffered. To minimize the number of cable wires and signal repeaters, the PIO expansion approach uses bi-directional lines and time-multiplexed data transmission. In this way, 32 lines are used to transmit a 256-bit-data word in either direction. A detailed logic design of the recommended PIO expansion philosophy was completed; three new PC boards were designed as part of this effort.

EVALUATION

The on-going program for the evaluation of parallel processing technology using the STARAN Associative Processor showed the necessity for interfacing other devices to STARAN. The Data Manipulator and Mass Memory were two items identified as desirable adjuncts to the Associative Processor. To support the interfacing of such devices, the STARAN I/O capability needed to be defined and expanded.

This effort developed a philosopy for providing wide bandwidth I/O channels for the STARAN machine.

The proposed design philosophy will minimize the cost of interfacing new devices without sacrificing I/O performance and simplify the future expansion of the parallel processing capability at RADC.

MURRAY KESSELMAN
Project Engineer

SUMMARY

OBJECTIVE

The objective of this project was to develop a comprehensive philosophy of input/output (I/O) for the STARAN* associative processor located at RADC. This included the specification of existing interfaces and the design and specification of a parallel I/O (PIO) capability compatible with the overall design philosophy of the STARAN computer.

EXISTING I/O CHANNELS

General

Three I/O channels currently exist in the STARAN computer located at RADC:

1. Buffered input/output (BIO)
2. Direct memory access (DMA)
3. External function (EXF)

The BIO and DMA channels were originally designed to be expandable; that is, interface boards exist that supply the channel signals for the device and also repeat them for the next user. Therefore, no system design was required to allow easy interfacing to the BIO and DMA channels by external users.

BIO Channel

The BIO channel allows external devices to access the STARAN control memory. The BIO control of reading and writing STARAN memory is identical to other STARAN elements accessing memory. All devices currently connected to the BIO channel of the STARAN at RADC use the standard channel interface boards. Therefore, an unused connection to the channel exists, and specification of the locations and pin-outs of all BIO signals was straightforward.

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DMA Channel

The DMA channel allows STARAN to read and write an external device. A device connected to the DMA channel is addressed as an integral part of STARAN control memory. The interface to the Honeywell Information System (HIS) 6180 does not use the standard DMA daisy chain boards to access the channel; therefore, no unused DMA port exists at RADC. Because of space limitations at the HIS 6180 interface, it is anticipated to interrupt the DMA channel nearer to its source. A set of interface boards would be installed to split the DMA channel into the existing channel and a port available for expansion. The location of DMA signals were specified as being at the proposed interface boards.

EXF Channel

The EXF channel facilitates coordination among the different STARAN elements, provides for special functions, and simplifies housekeeping, maintenance, and test functions. By issuing external function codes to the EXF logic, an external device can interrogate and control the status of any EXF element. The EXF channel was not designed to be expandable beyond the current system at RADC. Thus, methods were developed to allow external users to use the EXF channel.

Based on the design of other interfaces that required the use of EXF, two channels were designed. The first is a complete channel where the external device may either be controlled via EXF codes or issue EXF commands or both. This channel would require the daisy chaining of 44 signals, which can be accomplished on two boards. The second proposed EXF channel would require the external user to drive only one signal and receive two signals; this channel would connect to a set of selectors that would pass a hard wired code to the EXF channel. In this way, an external user would be able to issue a single, fixed EXF code with a minimum of interconnections.

The detailed I/O specification covers the proposed interfacing methods as well as the capabilities of the current EXF channels.

PIO EXPANSION STUDY

General

GAC developed a parallel I/O (PIO) that provides the most flexible and cost-effective method of interfacing various devices with the RADC STARAN PIO unit. Three areas were covered as part of this PIO expansion investigation:

1. The first was to make a 1024-bit-wide path to the PIO accessible to external users.
2. The second covered the various methods of data distribution to external devices.
3. The third dealt with the methods by which data transfer to external PIO users can be controlled.

1024-Bit-Wide Data Path

Currently only 768 bits are available to peripheral devices. There are two restrictions to the problem of expanding this capability to a 1024-bit-wide data path: (1) a physical maximum of 38 card slots is available for this 1024-bit-wide channel; (2) an interface between the 32-bit PIO data bus and the PIO unit must be maintained.

The solution to this accessibility problem was to make the 256-bit port used by the PIO data bus interface accessible also to external users. The PIO data bus interface would either be incorporated in the data distribution channel to external devices or would be placed outside the PIO unit as an external device. The placement is based on the data distribution method chosen.

Data Distribution Methods

The investigation of data distribution methods centered on four parameters:

1. Buffered or unbuffered I/O
2. Daisy-chain or fan-out expansion
3. Time-multiplexed or parallel data transmission
4. Uni-directional or bi-directional lines

The unbuffered I/O was chosen because it provides block data transfers that are at least twice as fast as those provided by a buffered I/O. This is

the result of the elimination of one instruction in the typical transfer program loop. Buffers exist in the PIO cabinet between the PIO unit and the associative arrays; thus the inclusion of additional buffers between the PIO unit and external devices would not have added any flexibility.

The daisy-chain method of expansion was chosen for two reasons. First, when each device connecting to the PIO channel is constrained to repeat the channel, a much larger number of devices may be attached to the channel than if the PIO channel were fanned-out. Second, the amount of initial hardware to implement the expansion method would be much less for the daisy-chain approach than a fan-out approach. For example, the proposed daisy-chained expansion method requires 33 new printed circuit (PC) boards; however, fanning out the 1024-bit-wide channel would require approximately 230 new PC boards.

Time-multiplexed data transmission was chosen because of the large reduction of cabling required to connect to the PIO channel. Instead of 256 signals in each direction, time-multiplexing uses just 32 signals per direction. This is a great savings in hardware to the external device supplier not only in the number of wires per cable but also in the number of repeaters he must provide for daisy chaining. Another advantage of the time-multiplexed method is that it allows the PIO data bus interface to be included within the PIO unit. This reduces the amount of hardware needed to implement the expansion philosophy.

Simultaneous reading and writing of the same device or array across the PIO channel is not permitted by the PIO control unit. Therefore, bi-directional data lines can be used. This would again reduce the amount of cabling required by a PIO channel user.

In summary, the recommended expansion method is the 32-bit time-multiplexed, bi-directional, unbuffered, daisy-chain design.

PIO Channel Control

The investigation developed methods by which data transfer to external PIO users are controlled. Existing control of PIO data transfers is designed to manipulate associative arrays. This control is not applicable to a special peripheral attached to the PIO for two reasons. First, the arrays are

asynchronous devices; i.e., there is no handshaking between the arrays and the controller. Second, there are far too many address lines, those intended to select associative memory words and those for flip constants.

The lack of handshaking capability prevents an external device from delaying the next transfer. The recommended control path includes (1) a single handshaking path, (2) a direction of transfer line, (3) four enable bits specifying the active PIO port/ports, and (4) the output of a 16-bit general purpose control register. The control port also includes two clock lines used to synchronize the transfer of 32-bit bytes of data.

PIO EXPANSION DESIGN

The logic design for three new printed circuit boards was performed as part of the final phase of the development of a PIO expansion philosophy. The first board would handle the control interface between the PIO control unit and external users of the PIO channel. The second board would multiplex three 256-bit ports into three 32-bit I/O channels. The third board would perform the same function as the second and also provide the interface to the PIO data bus.

Only one control type PC board would be used per system, 24 standard multiplexer boards would be required, and 8 multiplexer and data bus interface boards would be needed per system. This total of 33 boards compares favorable with the 38-board slots currently available in the RADC STARAN.

PREFACE

This report was prepared by Goodyear Aerospace Corporation (GAC), Akron, Ohio, under USAF Contract F30602-76-C-0240. This work was sponsored by the Air Force Systems Command, Rome Air Development Center, N.Y. The report covers work that was started 9 April 1976 and completed 9 August 1976. The contractor's number for this report is GER-16378.

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SECTION I

INTRODUCTION

1.1 OBJECTIVE

The objective of this effort has been to develop a comprehensive philosophy of input/output (I/O) for the STARAN* associative processor at Rome Air Development Center (RADC), N.Y. This has included (1) the specification of existing interface channels and (2) the design and specification of a parallel I/O (PIO) capability compatible with the overall design philosophy of STARAN.

1.2 BACKGROUND

RADC acquired a STARAN parallel processing computer in March 1973. Initially, this computer was envisioned as a self-contained system. Subsequently, RADC decided that STARAN could be best utilized as part of an overall computational facility. At the same time, the concept of a reconfigurable computer system facility was developed at RADC, and its implementation was started. This facility is to be used to develop techniques for the evaluation of various advanced computer architectures as they relate to specific Air Force problems. STARAN will become a vital part of this facility.

As the use of STARAN expanded at RADC, the need for additional parallel, computational support became evident. For this purpose, a hardware data manipulator and a mass memory are being developed by RADC. The addition of these devices makes it evident that the I/O capability of STARAN, as delivered to RADC, is inadequate to meet the new overall system requirements.

RADC desires that the most efficient use be made of the STARAN I/O ports. The first step in accomplishing this is to fully specify the operational characteristics of the current STARAN I/O ports. This allows the most efficient, standard interface connections possible to STARAN. Following this, the design and subsequent specification of a PIO interface has been performed to allow maximum data transfer rates between STARAN arrays and various high bandwidth peripheral devices being developed at RADC.

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*TM, Goodyear Aerospace Corporation, Akron, Ohio.

SECTION II

EXISTING I/O PORTS

2.1 GENERAL

Three I/O channels currently exist in the STARAN associative processor (AP) located at RADC:

1. Buffered input/output (BIO)
2. Direct memory access (DMA)
3. External function (EXF)

2.2 BUFFERED INPUT/OUTPUT (BIO) CHANNEL

The BIO channel is a 32-bit-wide, bi-directional I/O port on the STARAN computer. This port allows an external device to access all the STARAN control memory except for the high-speed page memories. The BIO channel is a daisy-chained I/O channel. Each device utilizing the BIO channel should take the signals for its own use and also repeat them for the next user.

The interface specification for BIO includes a complete description of the operation and the connecting techniques of the channel. Also covered in the BIO specification are descriptions of (1) all logic signals and lines; (2) all timing information; (3) logic levels, drive, and loading requirements; (4) cable type and length restrictions; and (5) the channel action for various illegal conditions.

Each device currently connected to the STARAN BIO channel at RADC uses a set of standard channel interface boards. This assures that an unused port connection is available for external users. Thus the location and pin-outs of all BIO signals can be readily specified.

2.3 DIRECT MEMORY ACCESS (DMA) CHANNEL

The DMA channel is a 32-bit-wide, two-directional I/O port on the STARAN computer. This port allows STARAN to access external device as an integral part of its control memory structure. The DMA channel is under STARAN control, with STARAN initiating the transfer of either data or command words over the channel. A device placed on the DMA channel is required to recognize its specifically assigned addresses and respond properly

to the handshake signals within a defined period of time. The DMA channel is a daisy-chained I/O channel. Each device utilizing the DMA channel should take the signals for its own use and also repeat them for the next user.

As with BIO channel, the DMA interface specification includes complete descriptions of the DMA channel operation, DMA signals and lines, and handling of error conditions. The DMA I/O specification also contains all timing information, logic levels, drive and loading requirements, and cable type and length restrictions.

Currently there is no unused DMA port in the STARAN at RADC. The Honeywell Information System (HIS) 6180 interface does not use the standard DMA daisy-chain boards to access the channel. Thus, additional hardware will have to be installed to allow external users to connect to DMA. Because of space limitations at the HIS 6180 interface, it is desirable to interrupt the DMA daisy chain nearer to its source. There, a set of standard interface PC boards would be installed to split the DMA channel into the existing daisy chain and a port available for expansion.

Figure 1A shows the DMA channel as it currently exists at RADC, and Figure 1B shows the proposed change to the daisy chain to allow for expansion. This expansion would involve the addition of components in the STARAN AP control cabinet; namely, a DMA interface (four PC boards), a differential driver/receiver (two PC boards), backpanel wiring, and one cable. The expansion would allow external devices to connect to the DMA channel. The location of DMA signals were specified at the spare port of the proposed interface boards.

2.4 EXTERNAL FUNCTION (EXF) CHANNEL

2.4.1 General

Figure 2A shows the current STARAN EXF channel as it currently exists at RADC. Figures 2B and 2C show two expansion methods that have been developed by Goodyear Aerospace.

2.4.2 Current EXF Channel (Figure 2A)

The current EXF channel enables the AP control, sequential controller, or external devices to control STARAN operation. The EXF logic facilitates

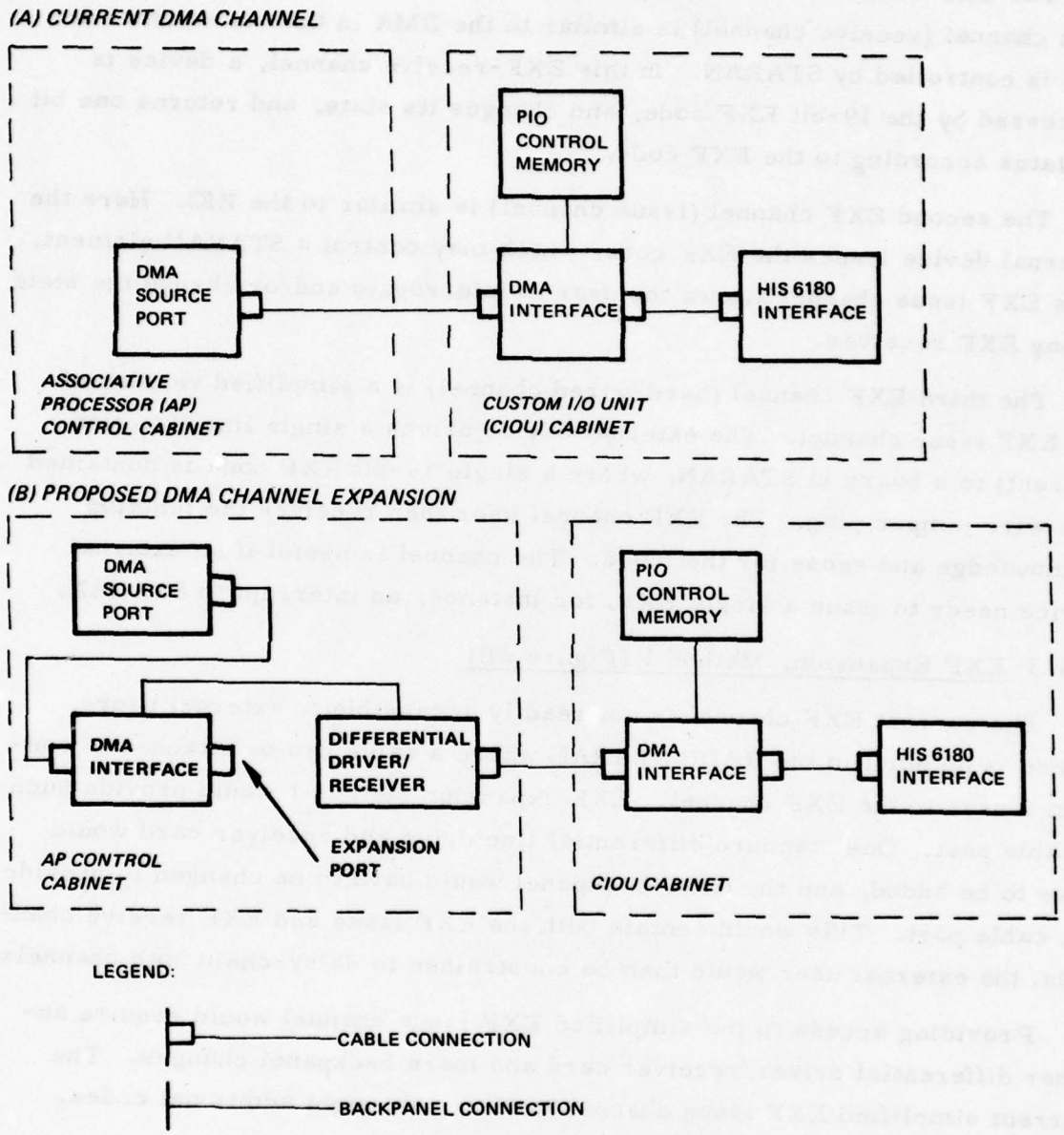


Figure 1. Current and Proposed DMA Channels for RADC STARAN Associative Processor

coordination among the different STARAN elements, provides for special functions, and simplifies housekeeping, maintenance, and test functions. By issuing external function codes to the EXF logic, an EXF issuing device can interrogate and control the status of any EXF element.

The EXF channel can be thought of as three separate channels. The first channel (receive channel) is similar to the DMA in that an external device is controlled by STARAN. In this EXF-receive channel, a device is addressed by the 19-bit EXF code, and changes its state, and returns one bit of status according to the EXF code.

The second EXF channel (issue channel) is similar to the BIO. Here the external device issues the EXF code, which may control a STARAN element. This EXF issue channel allows the user to interrogate and/or change the state of any EXF receiver.

The third EXF channel (hard-wired channel) is a simplified version of the EXF issue channel. The external device drives a single line (function present) to a board in STARAN, where a single 19-bit EXF code is contained in a wire jumper plug. The EXF channel user then receives the function acknowledge and sense for that code. The channel is useful if an external device needs to issue a single EXF; for instance, an interrupt to STARAN.

2.4.3 EXF Expansion, Method 1 (Figure 2B)

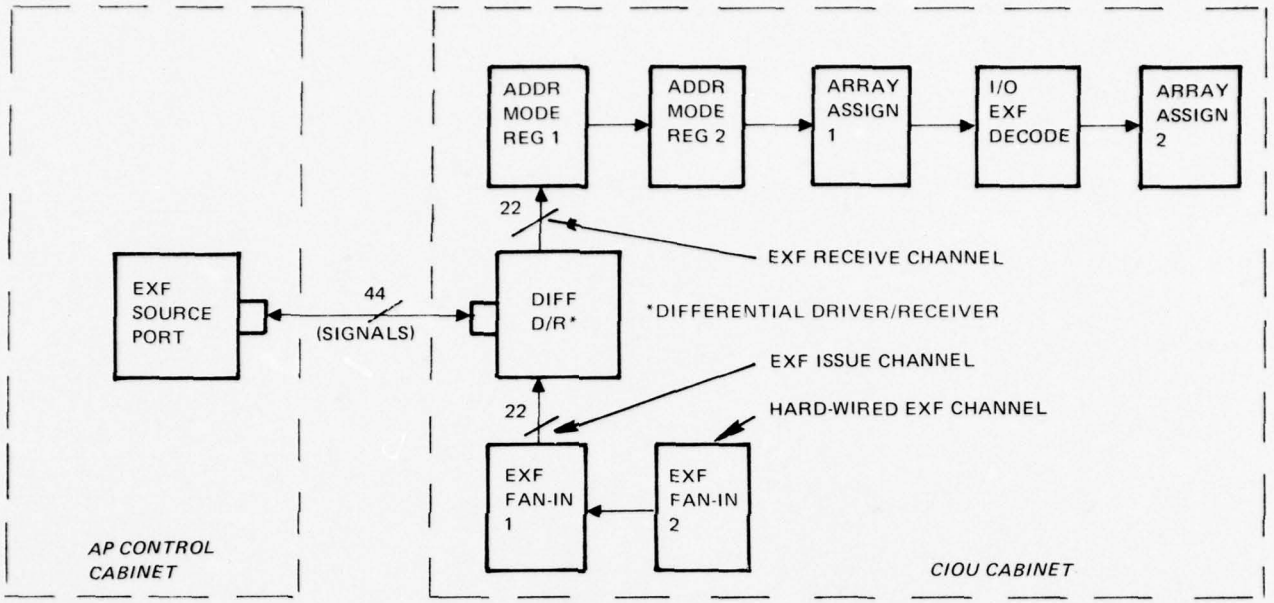
The current EXF channel is not readily accessible to external users. There is no point in the RADC STARAN where a cable can be attached to connect a user to the EXF channel. EXF expansion Method 1 would provide such a cable port. One standard differential line drive and receiver card would have to be added, and the CIOU backpanel would have to be changed to provide the cable port. This would contain both the EXF issue and EXF receive channels; the external user would then be constrained to daisy-chain both channels.

Providing access to the simplified EXF issue channel would require another differential driver/receiver card and more backpanel changes. The current simplified EXF issue channel handles only eight additional codes.

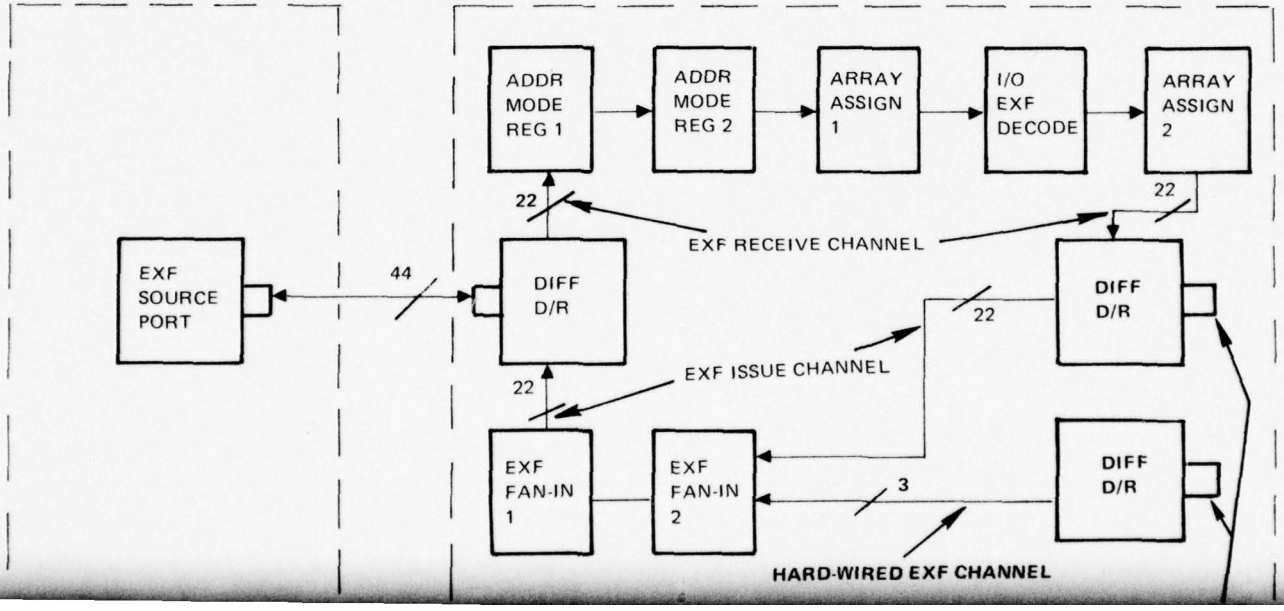
2.4.4 EXF Expansion, Method 2 (Figure 2C)

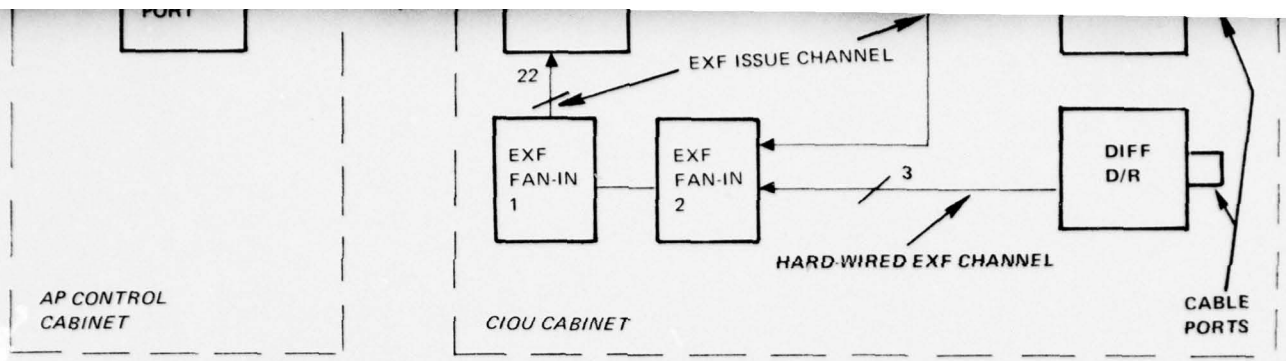
Goodyear Aerospace has also developed a preliminary design for expandable EXF channels that is consistent with the overall STARAN philosophy.

(A) CURRENT EXF CHANNEL



(B) PROPOSED EXP CHANNEL EXPANSION, METHOD 1





(C) PROPOSED EXP CHANNEL EXPANSION, METHOD 2

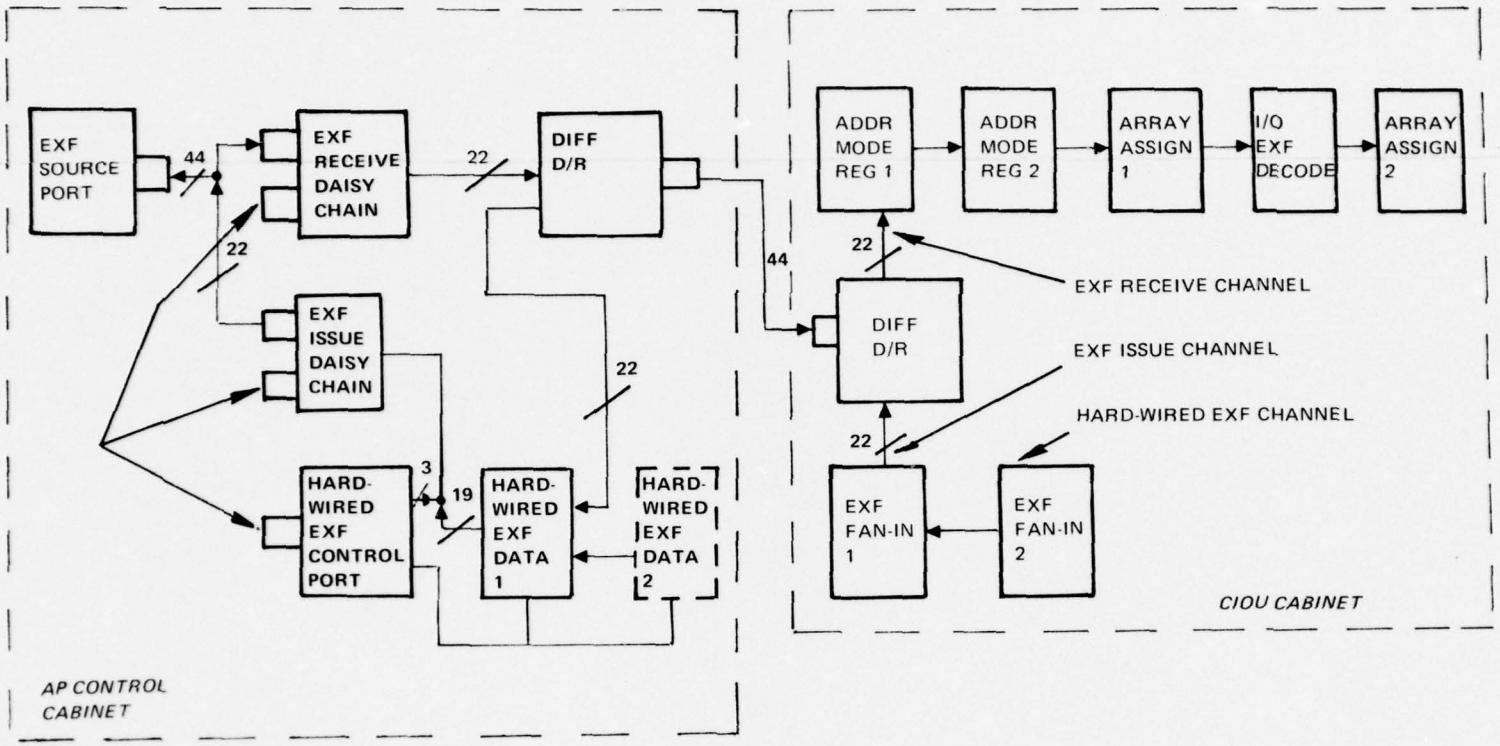


Figure 2. Current and Proposed EXF Channels for RADC STARAN Associative Processor

This design, identified as expansion Method 2, creates four new PC boards:

1. The first board provides the daisy-chain function for the EXF issue channel.
2. The second board daisy-chains the EXF receive channel.
3. The last two boards handle the jumper-wired EXF code channel. One of these boards accepts 12 sets of control lines from external users; it resolves any conflicts between the twelve users and selects the corresponding EXF code. The other board for the EXF code channel accepts six wire-jumper plugs for the EXF codes.

This philosophy provides for minimum hardware within an external EXF user. A device need only connect to the particular channel in which the user is interested.

Implementation of Method 2 would require the installation of at least three PC boards into the STARAN AP control cabinet. Two more boards would be needed to implement the simplified EXF issue channel. This expansion would interrupt the EXF channel near its source. Thus, the slew and delay in the channel would be minimized over a connection at the end of the EXF devices within CIOU cabinet.

The operating characteristics of the EXF channel are independent of the expansion method. Thus, the complete description of the channel operation and signals has been included in the interface specification. Also covered in the EXF I/O specification are (1) all timing information, (2) logic levels, drive and receive requirements, (3) cable type and length restrictions, and (4) a description of the channel action for various-illegal conditions. The location of EXF signals and a complete description of each expansion method are covered by the interface specification.

SECTION III

STUDY OF PIO EXPANSION

3.1 BACKGROUND

GAC has developed an I/O philosophy that provides a flexible, cost-effective method of interfacing various devices with the RADC STARAN PIO unit.

The STARAN PIO unit presently has eight PIO ports. Ports 0 through 3 are buffered ports and are tied to arrays 0 through 3, respectively. Port 7 is tied to the 32-bit PIO control data bus via a fan-in fan-out network. Ports 4 and 5 are wired for PIO buffer cards but are now unpopulated. Port 6 has been left unwired for the potential use of an external device, such as a parallel head disk system. At present, three PIO ports are available where external equipment could be connected.

RADC wants to interface a 1024-bit wide mass memory, a 64-bit wide data manipulator, and possibly other peripheral devices onto the PIO port structure. The addition of these devices would require more PIO ports than are now available. A PIO port expansion philosophy has been developed for the RADC STARAN facility. This philosophy provides for:

1. Capability of 1024-bit wide data paths to the PIO structure
2. Various methods of data distribution to external devices
3. Capability of synchronizing data transfers from the PIO structure

3.2 CAPABILITY OF 1024-BIT WIDE PATH

The first area covered by the PIO expansion investigation was how to make a 1024-bit-wide data path accessible to PIO. There are two restrictions on any solution to this problem: (1) a physical maximum of 38 card slots are available for this 1024-bit channel; (2) an interface between the 32-bit PIO data bus and the PIO unit must be maintained. The solution to this accessibility problem is to make the 256-bit port used by the PIO data bus interface accessible also to external devices.

The present method of implementing a PIO port uses 10 PC boards. Since incorporating four 256-bit ports by this method would require two more card slots than are available, some redesign must be done. By retaining the uni-directional, differential driver/receiver technology, the port buffer cards could be designed so that a port would be comprised of nine boards. This method would solve the card count restriction; however, the 32-bit PIO data bus interface would have to be placed outside the PIO cabinet. Various other data distribution methods would allow the PIO data bus interface to be included within the port 7 channel, and thus reduce the cost of implementation.

3.3 DATA DISTRIBUTION METHODS

3.3.1 General

The second item of the PIO expansion investigation covered various methods of data distribution to external devices. The four parameters of the distribution systems are:

1. Buffered or unbuffered I/O
2. Daisy-chain or fan-out expansion
3. Time-multiplexed or parallel-data transmission
4. Uni-directional or bi-directional lines.

3.3.2 Buffered-vs-Unbuffered I/O

Unbuffered ports were chosen because their block data transfer rates are half those for buffered ports. This is a result of the change from a two PIO instruction loop to a single instruction loop for data transfer control. In the following discussion, a typical software loop for a block transfer from an associative array memory to an external device using buffered PIO port is compared to the loop when the ports are unbuffered.

For the case when the PIO ports are buffered, it is assumed that the first 256-bit word of data is loaded into the PIO array buffer register and transferred to the buffer register corresponding to the external device's port. At this point, the loop is entered. The first instruction loads the PIO array buffer register from the array; it also triggers the transfer of data from the PIO unit to the device. The next instruction is not loaded until the external device has acknowledged the receipt of the data. Once loaded, the second instruction loads the device's PIO buffer register from the array buffer register.

After this instruction completed, the loop is repeated until all data have been transferred to the external device.

For the unbuffered case, again it is assumed that the initial 256-bit word is loaded into the PIO array buffer register. At this point, a one-instruction loop is entered. The instruction loaded into the instruction register is a load of the array buffer register from the associative array memory. But prior to the actual load of the buffer, the data currently in the buffer are transferred to the port used by the external device, and the transfer to the device is initiated. Once the external device has acknowledged the receipt of these data, the load of the array buffer register takes place and the loop continues. Thus, for equal length blocks of data, approximately half the number of instructions have to be fetched and executed if the ports are unbuffered.

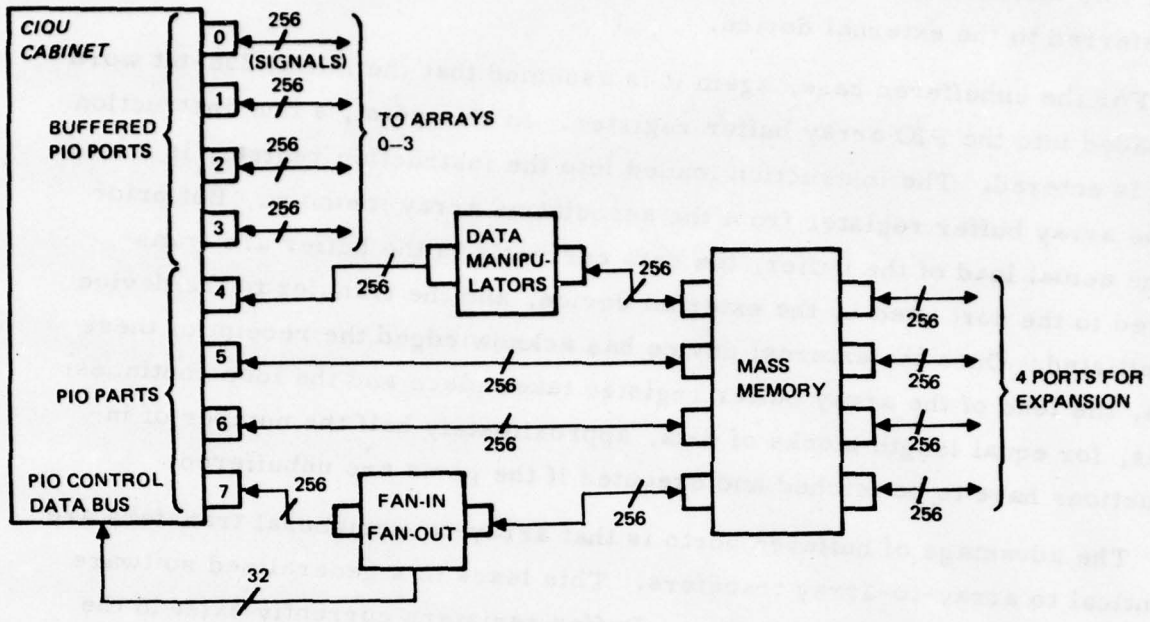
The advantage of buffered ports is that array-to-peripheral transfers are identical to array-to-array transfers. This leads to a generalized software package handling all PIO transfers. Buffer registers currently exist in the array ports between the PIO unit and the associative arrays. Thus the inclusion of additional buffers between the PIO unit and the external channels would not add any flexibility.

3.3.3 Daisy-Chain vs Fan-Out Expansion

The proposed PIO philosophy uses the daisy-chain method of expansion (see Figure 3A). This method is attractive because of its nearly unlimited expansion capabilities. When each device connecting to the PIO channel is constrained to repeat the channel, a much larger number of devices may be attached to the PIO channel than if the fan-out expansion method was employed. Another advantage of the daisy-chain method is that it greatly reduces the amount of hardware required for implementation, as compared with the fan-out approach.

The fan-out expansion method (see Figure 3B) takes each of the four PIO ports designated for external use and reproduces them a fixed number of times. The fan-out approach reduces the peripheral supplier's hardware by eliminating the channel repeaters. Another advantage of this method is that the propagation delay between the external devices and the PIO ports is independent of

(A) DAISY-CHAIN EXPANSION APPROACH



(B) FAN-OUT EXPANSION APPROACH

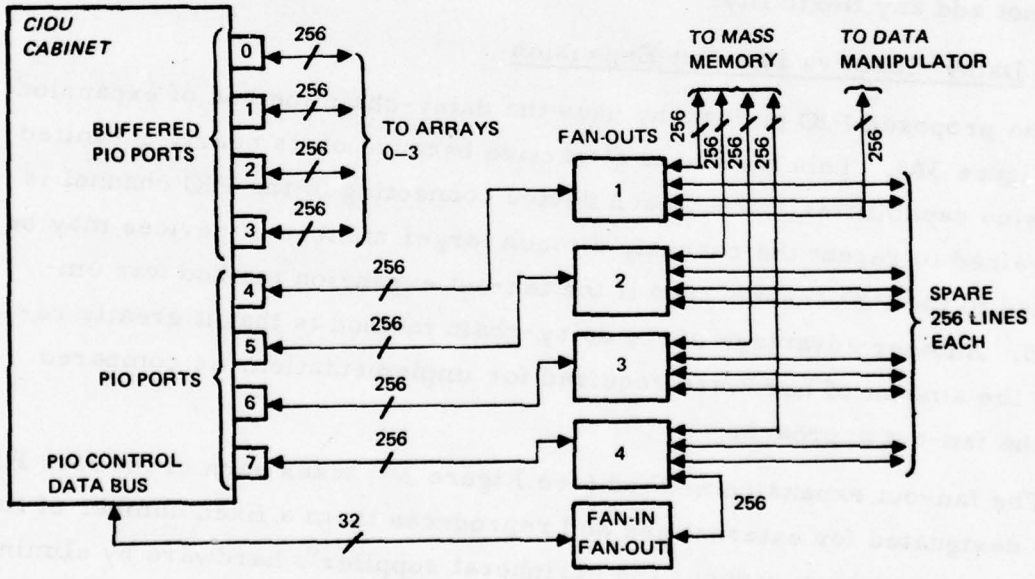


Figure 3. PIO Expansion Methods

the position of the device within the expansion system. The fan-out expansion method shown in Figure 3B uses a fan-out level of four.

The daisy chain method was selected primarily because of its low cost of implementation, expandability, and simplified control requirements. The proposed method requires 33 new PC boards, while the fan-out approach would use approximately 230 new boards.

3.3.4 Time-Multiplexed vs Parallel-Data Transmission

The advantages of parallel data transmission over time-multiplexing are threefold. First, the control logic is simplified; i.e., there is no need for byte clock generation and checking. Second, port hardware and interface hardware are simplified by the elimination of packing/unpacking circuitry. Third, lower data transfer rates are required.

However, parallel data transmission requires eight times the number of cable wires and at least four times the number of PC boards to daisy-chain the channel, as compared with time-multiplexing. A further advantage of time-multiplexed data transmission is that the PIO data bus interface can be included within the PIO unit. This reduces the amount of hardware needed to implement the expansion philosophy. The time-multiplexed approach was chosen because the reduction in hardware and costs far outweigh the minor simplification in logic design.

3.3.5 Uni-Directional vs Bi-Directional Lines

The PIO control unit does not have the capability to simultaneously read and write the same device or array. For this reason, uni-directional lines are not needed to transmit data for each direction. A bi-directional line transfers a data bit in either direction but not simultaneously. The use of bi-directional data lines reduces the amount of cabling required by a PIO channel user. The impact of this type of data lines is a minimal increase in the complexity of the peripheral's control logic.

Thus, the proposed PIO data-distribution expansion method is the 32-bit time-multiplexed, bi-directional, unbuffered, daisy-chain design. Figure 4 illustrates this expansion method.

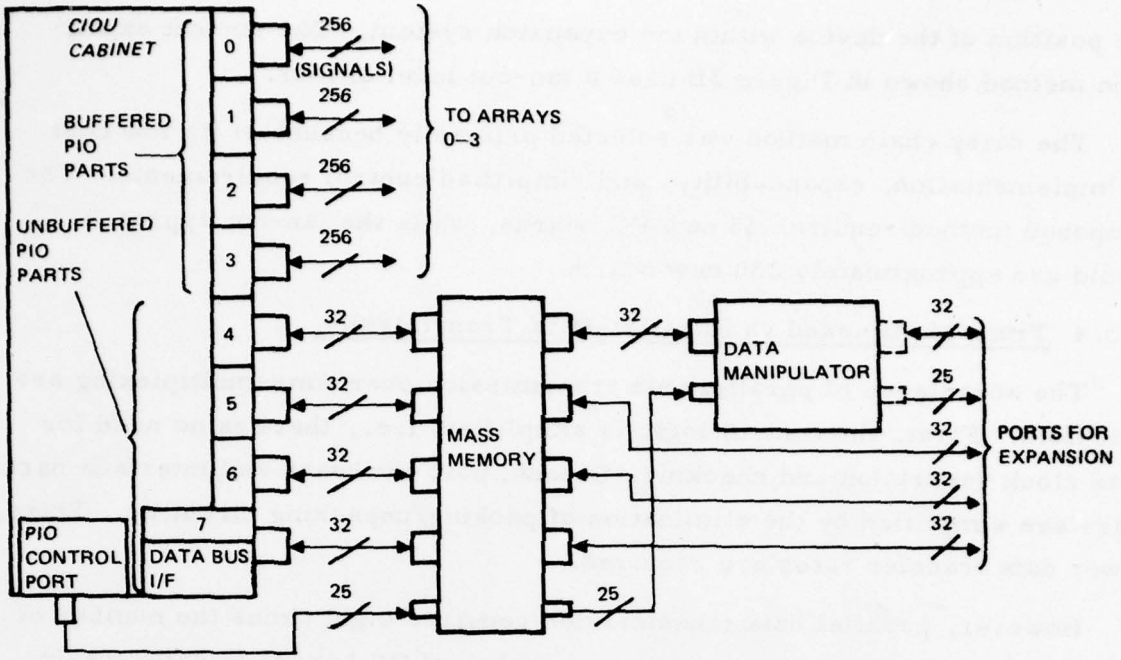


Figure 4. PIO Expansion Philosophy

3.4 PIO CHANNEL CONTROL

The third area investigated in the PIO expansion study was the capability of synchronizing data transfers from the PIO structure. The existing control of PIO data transfers is designed to manipulate the associative arrays. There are two reasons why this array control philosophy is not adaptable to control of PIO to external device transfers. First, there is no handshaking between the arrays and the controller; in the case of an external device, no handshaking capabilities bar the device from acknowledging the receipt of data. Second, there is an excessive number of address lines in the array control channel - those addressing the associative memory plus those controlling the flip network. Since these address lines are not readily programmed, their use as selection lines and general purpose control lines is minimal.

The proposed PIO control channel is one 25-line cable that includes the handshaking signals, the direction of transfer line, and four enable bits specifying which PIO ports are transferring. Also included are 16 bits of a

general purpose register and the clock lines used to synchronize the transfer of bytes of data. The driver of data is responsible for sending a pulse on the clock line with each byte. The receiver uses that pulse as a signal that data are available.

3.5 ADDITIONAL PARAMETERS OF PIO EXPANSION STUDY

Transfer rates were used in the choice between various PIO expansion approaches. As mentioned previously, these transfer rates are related to the number of instructions executed. A smaller number of instructions means lower transfer rates. Since the expansion approach recommended minimizes the transfer rate, it also minimizes the amount of software required to control the transfer. This minimization of programming is important since the instructions must be stored in the PIO control memory, which has limited storage.

The PIO control memory is currently a 512-word memory. Depending on the number of external devices on the PIO channel that are active during a program, this memory may not be of sufficient size. For example, the standard subroutine package that handle inter-array transfers via the PIO uses 115 words of the PIO control memory. The subroutine package for the parallel head disc, which is attached via an unbuffered port to the PIO at ETL, uses 212 words. This leaves 184 words available for another device driver or user programs. Thus if more than two devices are to be active during execution of a problem, their device drivers may have to be overlays. The least costly method to expand the PIO control memory would be to replace the storage boards with the newer ECL memory boards. These new boards would extend the memory from 512 words to 4096 words.

The recommended approach for expansion of the PIO channel is not compatible with the newly developed STARAN series E. The decision to waive compatibility was based on the complexity of the hardware required to modify the existing CIOU.

The STARAN E model provides a highly flexible I/O system. This STARAN E can support simultaneous bi-directional data transfers and can be either the initiator or receiver of the transfer. This allows the I/O device to initiate transfers by supplying array number, start address, and

word count. The CIOU system at RADC is designed for the uni-directional transfer of data, with the CIOU being the transfer initiator or supervisor.

To provide CIOU compatibility of the RADC system with the STARAN E series would require extensive modification of the CIOU hardware. Making these modifications would needlessly increase hardware cost and volume.

3.6 SUMMARY OF PIO EXPANSION STUDY

The hardware required and the costs involved in the implementation of the PIO expansion methods studied were deciding factors in the choice of the recommended approach. Table I compares the hardware required for these expansion methods and also shows the cost factors. In the table, each expansion method is identified according to the data-distribution option used, and includes the hardware required for data distribution as well as for a 1024-bit-wide data path and control logic.

The cost factors in Table I are normalized numbers in which the recommended PIO expansion method is used as a reference. This recommended method, shown in the first column of the table, uses a 32-bit multiplexed, bi-directional, unbuffered, daisy-chain data-distribution design.

TABLE I. PIO EXPANSION COMPARISON

Hardware and cost	PIO expansion method (grouped by data distribution option)					
	Daisy-chain, 32-bit time multiplexed, bi-directional, unbuffered	Daisy-chain, 32-bit time multiplexed, uni-directional, buffered	Daisy-chain, parallel data, bi-directional, unbuffered	Daisy-chain, parallel data, uni-directional, buffered	Fan-out, parallel data, bi-directional, unbuffered	Fan-out, parallel data, uni-directional, buffered
PC board designs	3	3	3	3	5	6
Required PC boards	33	33	33	61	229	232
Required cables	-	-	-	2	5	5
Required cabinets	-	-	-	-	1	1
Required backpanels	*	*	*	1+*	6+*	7+*
Normalized fabrication cost factor	1.0	1.0	1.0	1.6	4.5	5.0
Normalized installation and checkout cost factor	1.0	1.0	1.1	1.5	4.5	5.1
Normalized interfacing cost factor	1.0	1.5	4.4	8.7	3.0	5.4

*Rework of four existing PIO nests for all approaches.

SECTION IV

DESIGN OF PIO EXPANSION

4.1 GENERAL

Under this contract, Goodyear Aerospace has completed a detailed logic design of the recommended PIO expansion method. Three PC board types are required to implement the design: (1) the port multiplexer for use in PIO ports 4, 5, and 6; (2) the port 7 multiplexer, which contains the PIO data bus interface; and (3) the PIO port expansion control board. GAC has also provided a detailed specification of the interface expansion method. This I/O specification covers the operation of the channel, signal descriptions, logic levels including drive and loading requirements, cable type and length restrictions, and preliminary timing diagrams. Since no hardware was produced under this contract, the exact signals locations could not be specified.

4.2 LOGIC DESIGN

4.2.1 General

The port multiplexer board and the port 7 multiplexer board are nearly identical. The only difference is the inclusion of the 32-bit PIO data bus interface on the port 7 multiplexer. The major components of these boards are an 8-bit shift register and a 1-of-8 data selector. These elements handle the packing/unpacking of the 256-bit AP words. Shift registers are used rather than data distributors because of the reduction in the number of required control lines. Each PIO port is comprised of eight of the corresponding type boards. Thus each board contains 32 bits of the 256-bit-wide path and 4 bits of the 32-bit-wide paths.

Schematic diagrams for the PIO port multiplexer board, the PIO port 7 multiplexer board, and the PIO port expansion control board are shown in Appendix A.

The PIO port expansion control board serves a dual function. It controls the PIO port multiplexers and PIO channel transfers, and it is also the cable connection point for the PIO control channel. The PIO port expansion control board can b- analyzed from the standpoint of its three sections: (1) 16-bit

general purpose PIO control register, (2) handshaking logic, and (3) multiplexing logic.

4.2.2 Sixteen-Bit General Purpose PIO Control Register (PIOCR)

The 16-bit general purpose PIOCR was incorporated to be used for device selection or command and status. The PIOCR replaces the PIO interrupt mask register in the PIO data bus. The PIO interrupt mask register can be eliminated because the PIO control module is not interruptable and the register is elsewhere unused.

The advantage of connecting the PIOCR to the PIO data bus is that the PIO control module can access it as one of its standard registers. However, because the PIOCR replaces the PIO interrupt mask, the PIOCR cannot be stored directly into STARAN control memory. If this operation is attempted, a SWAP PSW instruction will be performed. This instruction will store both the PIO program counter and the PIOCR at the address specified within the instruction and load both from that address plus one. Therefore, to store the PIOCR into memory, it must first be loaded into intermediate register, and then that register must be stored into memory.

The three least significant bits of the PIOCR are used as error flags set by various illegal conditions on the PIO channel. The least significant bit is set when an external device returns its handshake signal before the PIO has sent the last byte of data. The next to least significant bit is set when an external device returns its handshake signal before it has sent the eighth byte of data to the PIO. The third error bit is set when no handshaking signal is returned within 20 milliseconds.

4.2.3 Handshaking Logic

The second section of the PIO port expansion control board handles the handshaking processes. The PIO port expansion control board receives information from the instruction register and parts of the instruction execution control logic. When this information signifies that activity is to take place on the PIO channel to external users, the PIO port expansion control board issues a handshaking signal, CONTINUE OUT. Along with this signal, the control board sends a direction of transfer line and four enable lines indicating which PIO ports are selected to participate in the transfer. After all

eight bytes of data have been transferred, the external device raises its handshake line, CONTINUE IN. Upon receipt of CONTINUE IN, the control board lowers CONTINUE OUT and allows PIO instruction execution to continue. In the case when data are being received by the PIO, the receipt of CONTINUE IN also causes the load of the selected PIO array buffer registers. When the 20-millisecond time-out expires prior to the receipt of CONTINUE IN, an error flag is set, and the CONTINUE IN is generated internal to the PIO port expansion control board so that instruction execution can continue.

4.2.4 Multiplexing Logic

The third section of the PIO port expansion control board contains the logic that controls the multiplexing of data. The multiplex control logic includes the clock generation, receiving, and counting circuitry. Here, dependent on the direction of the transfer, either clock pulses are generated and sent to the external device, or clock pulses are received from the external device. These clocks trigger a counter that contains the number of the particular byte being transferred. This counter is also used in the check procedure. If the CONTINUE IN line should be received before all eight bytes have been transferred, an error bit will be set.

After completion of this logic design effort, a preliminary timing analysis was performed. Minimal delays within the external device were assumed. The results of this analysis are as follows:

1. For a transfer from the STARAN to an external device, the cycle time will be approximately 500 nanoseconds.
2. In the other direction, the cycle time will be about 600 nanoseconds; this is because the data transferred from the external device must be loaded into the PIO array buffer register and then into the array.

4.3 IMPLEMENTATION

To incorporate this PIO expansion method into the STARAN computer at RADC would require the purchase of 33 PC boards: 24 PIO port multiplexers, 8 PIO port 7 multiplexers, and 1 PIO port control board. The backpanel wiring in the custom interface cabinet would have to be changed. Ports 4, 5, and 7 of the PIO data switch network would have to be rewired to accept the

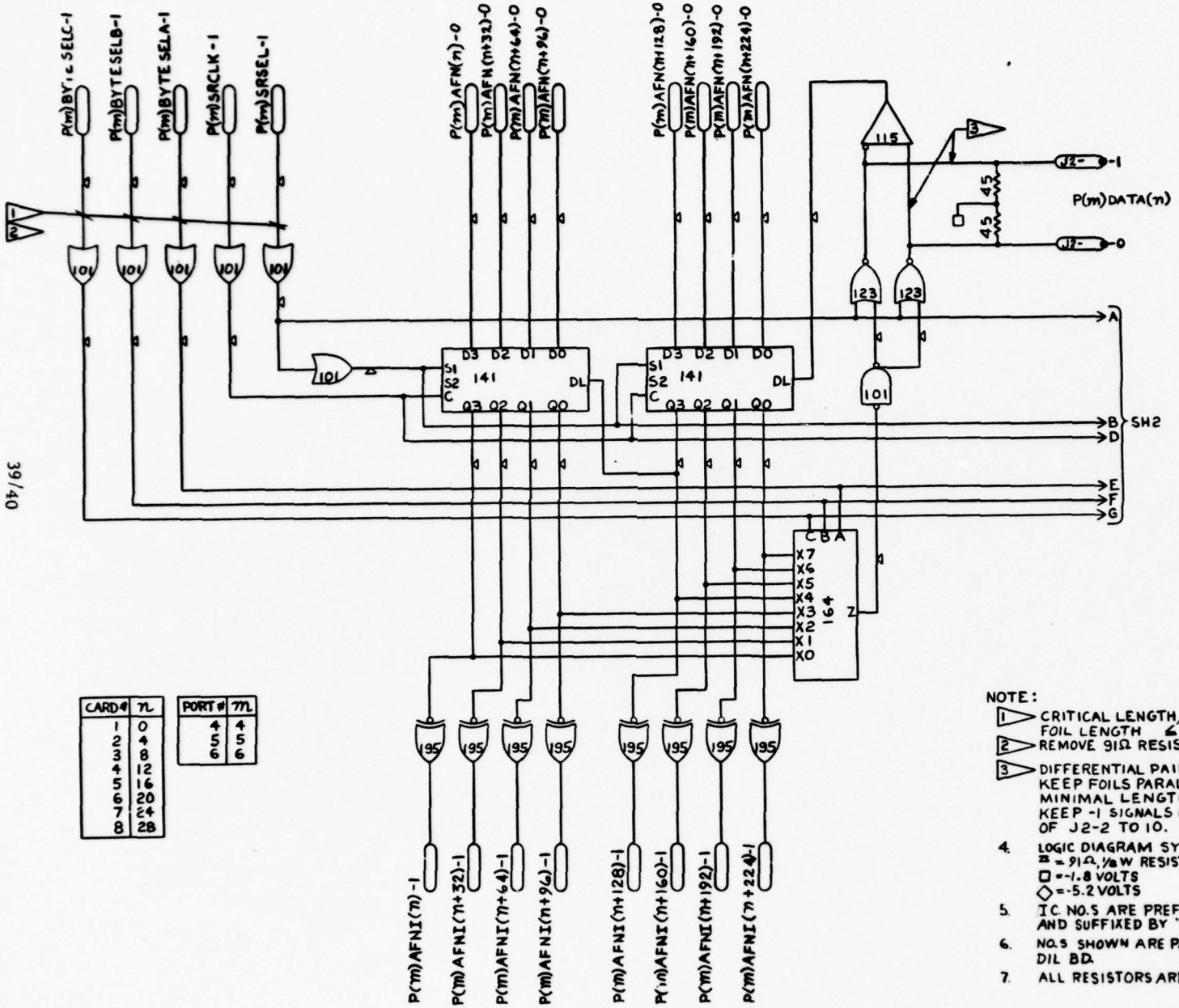
multiplexer boards. Since port 6 is currently unwired, only the connecting wires would have to be added to incorporate the port 6 channel. Additional changes to the backpanel wiring would be needed for the PIO channel control port. The total of 33 PC boards that would be required compares favorably with the 38 board slots currently available in the custom interface cabinet at RADC.

No additional cabling, power supplies or cabinets would be required, The implementation is contained within the existing STARAN equipment.

APPENDIX A

PIO EXPANSION SCHEMATIC DIAGRAMS

Included in Appendix A are the schematic diagrams for three PC boards that were designed as part of the study resulting in a recommended PIO expansion method: (1) PIO port multiplexer board, (2) PIO port 7 multiplexer board, and (3) PIO port expansion control board.



CARD #	n
1	0
2	4
3	8
4	12
5	16
6	20
7	24
8	28

PORT #	m
4	4
5	5
6	6

NOTE:

1. CRITICAL LENGTH, KEEP FOIL LENGTH ≤ 2 INCHES
2. REMOVE 91Ω RESISTORS ON 103 ASSY
3. DIFFERENTIAL PAIR. KEEP FOILS PARALLEL AND MINIMAL LENGTH. KEEP -1 SIGNALS ON EVEN PINS OF J2-2 TO 10.
4. LOGIC DIAGRAM SYMBOLS
   ▭ = 91Ω, ⅛W RESISTOR TO -1.8V
   □ = -1.8 VOLTS
   ◇ = -5.2 VOLTS
5. IC NOS ARE PREFIXED BY "MC10" AND SUFFIXED BY "L"
6. NOS SHOWN ARE PAD NOS ON STD DIL BD.
7. ALL RESISTORS ARE 91Ω, ⅛W

Figure A-1. PIO Port Multiplexer PC Board (Sheet 1 of 3)

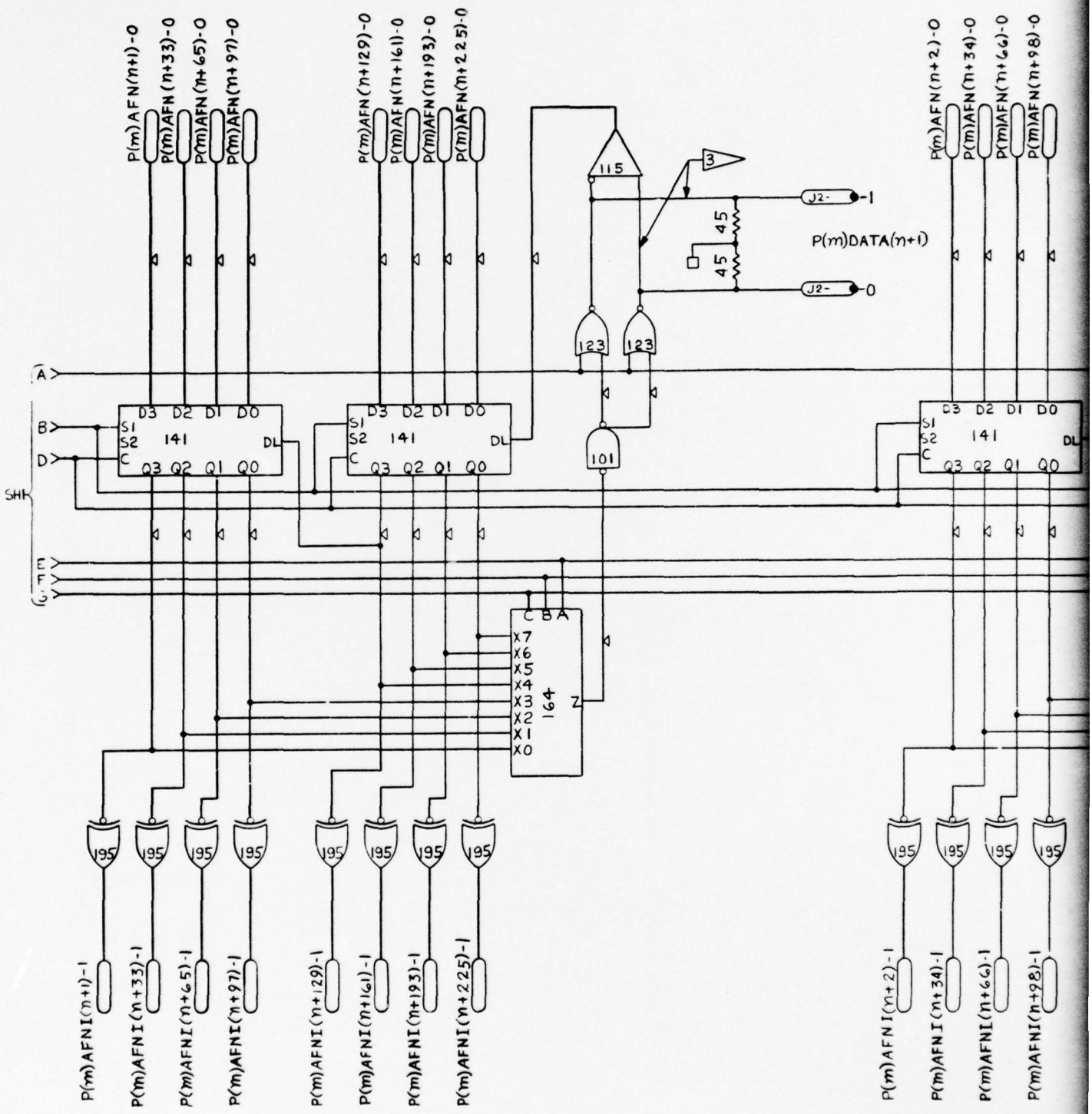

P(m)AFN(n+1)-0
P(m)AFN(n+33)-0
P(m)AFN(n+65)-0
P(m)AFN(n+97)-0
P(m)AFN(n+129)-0
P(m)AFN(n+161)-0
P(m)AFN(n+193)-0
P(m)AFN(n+225)-0
P(m)AFN(n+2)-0
P(m)AFN(n+34)-0
P(m)AFN(n+66)-0
P(m)AFN(n+98)-0
115
3
J2-1
45
45
P(m)DATA(n+1)
J2-0
123
123
101
A
B
D
SHF
E
F
G
D3 D2 D1 D0
S1
S2
C
141
DL
Q3 Q2 Q1 Q0
C B A
X7
X6
X5
X4
X3
X2
X1
X0
164
Z
195
P(m)AFNI(n+1)-1
P(m)AFNI(n+33)-1
P(m)AFNI(n+65)-1
P(m)AFNI(n+97)-1
P(m)AFNI(n+129)-1
P(m)AFNI(n+161)-1
P(m)AFNI(n+193)-1
P(m)AFNI(n+225)-1
P(m)AFNI(n+2)-1
P(m)AFNI(n+34)-1
P(m)AFNI(n+66)-1
P(m)AFNI(n+98)-1

Figure A-

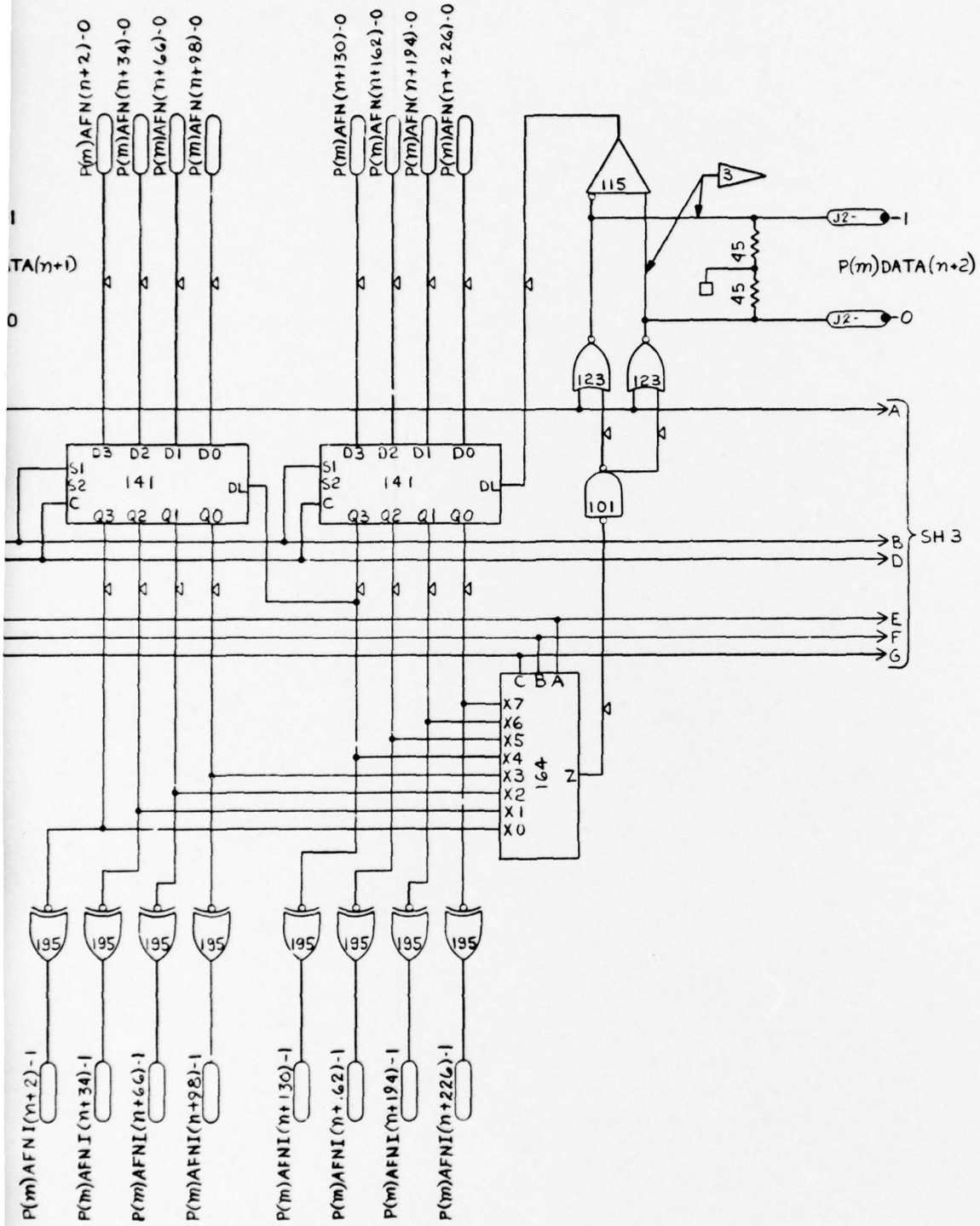


Figure A-1. PIO Port Multiplexer PC Board (Sheet 2 of 3) 41/42

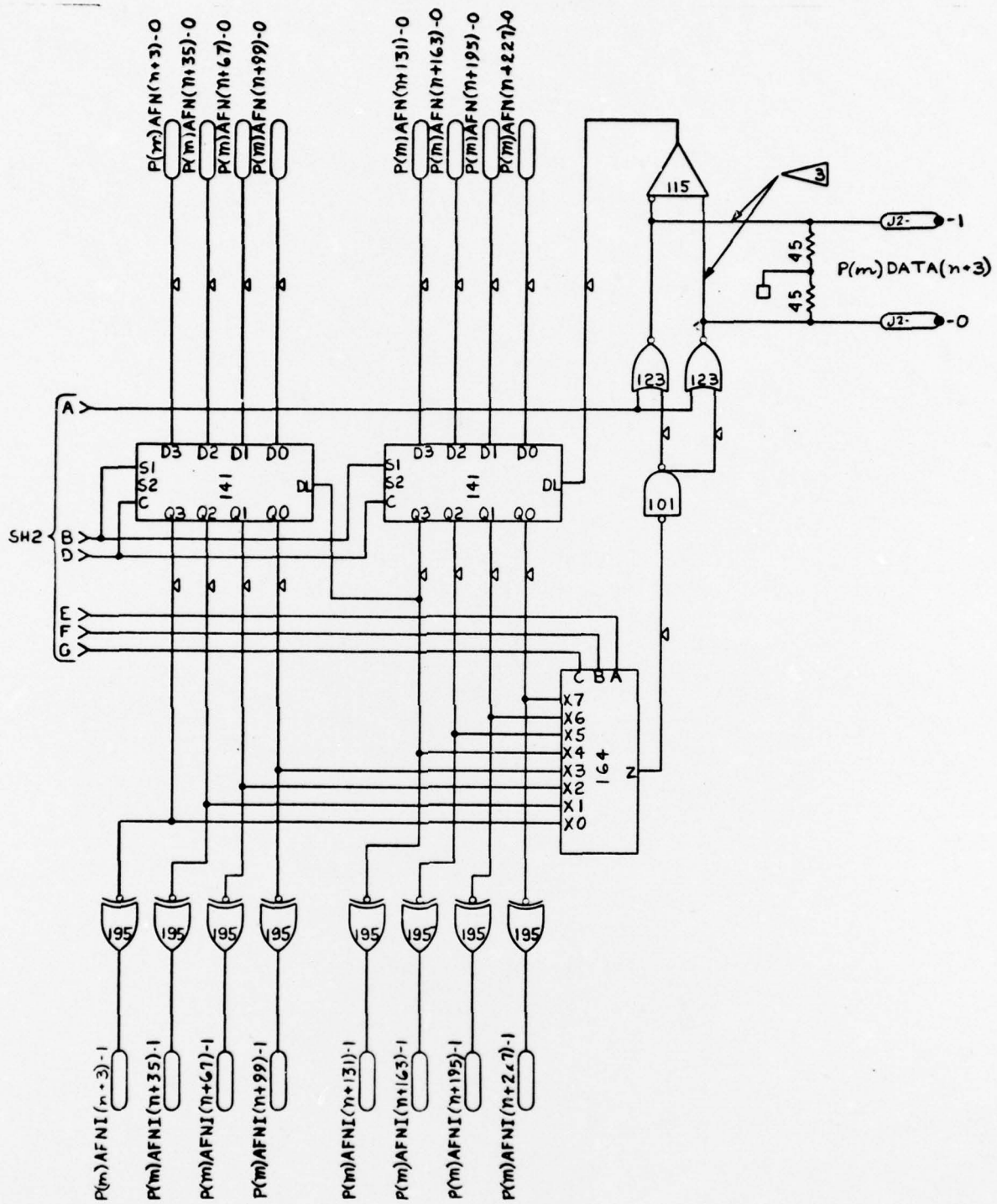


Figure A-1. PIO Port Multiplexer PC Board (Sheet 3 of 3)

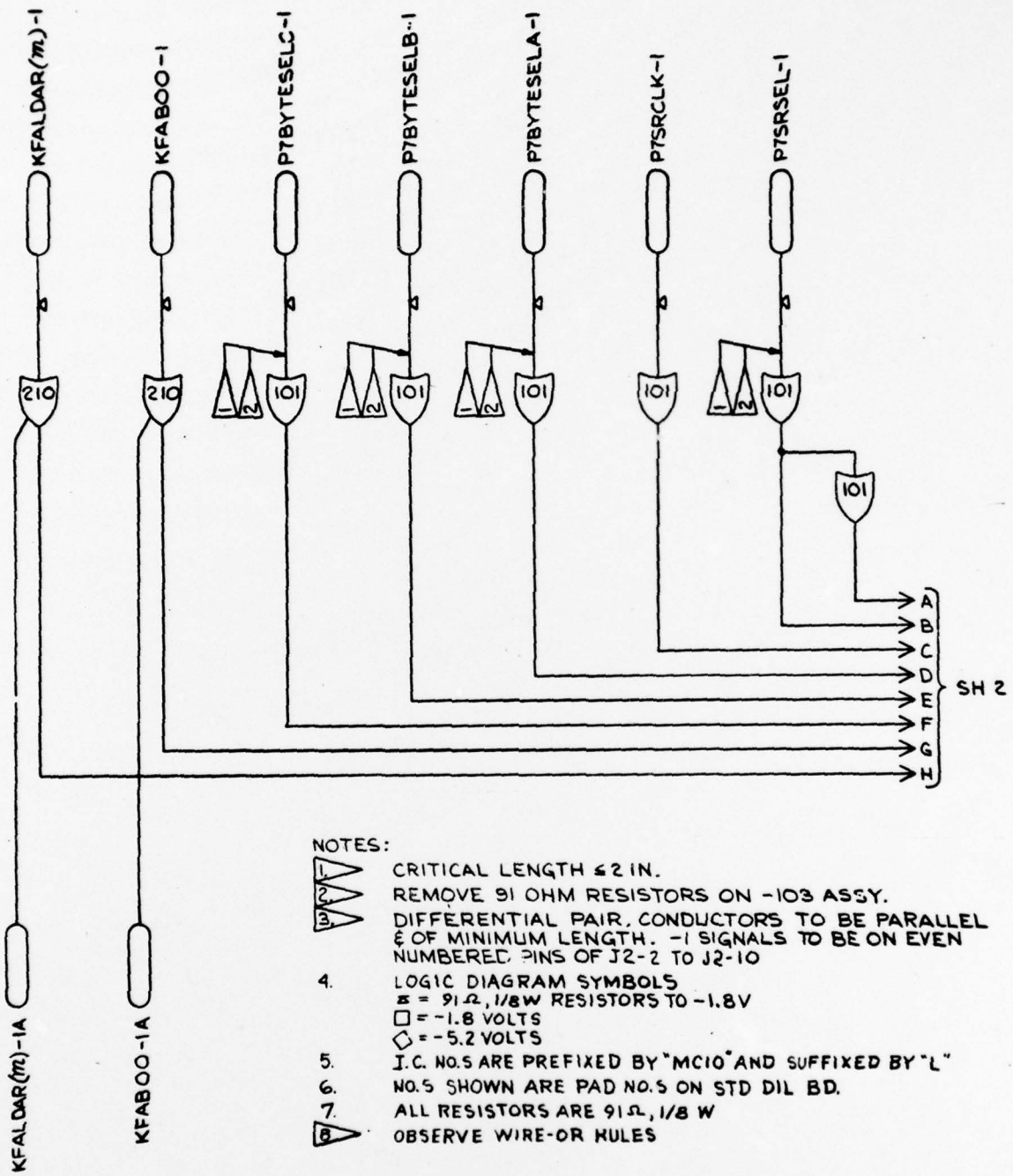


Figure A-2. PIO Port 7 Multiplexer PC Control Board (Sheet 1 of 5)

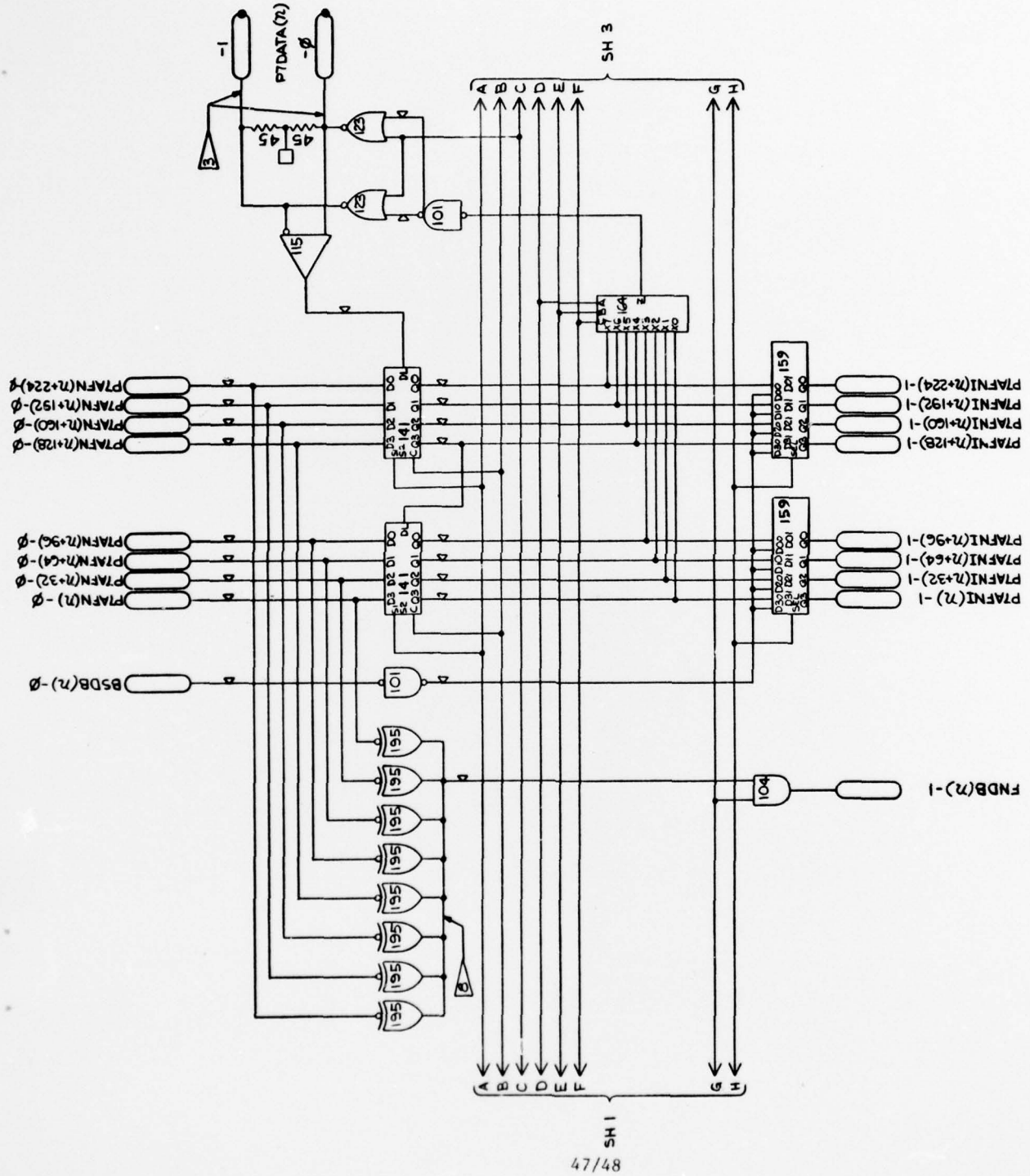


Figure A-2. PIO Port 7 Multiplexer PC Control Board (Sheet 2 of 5)

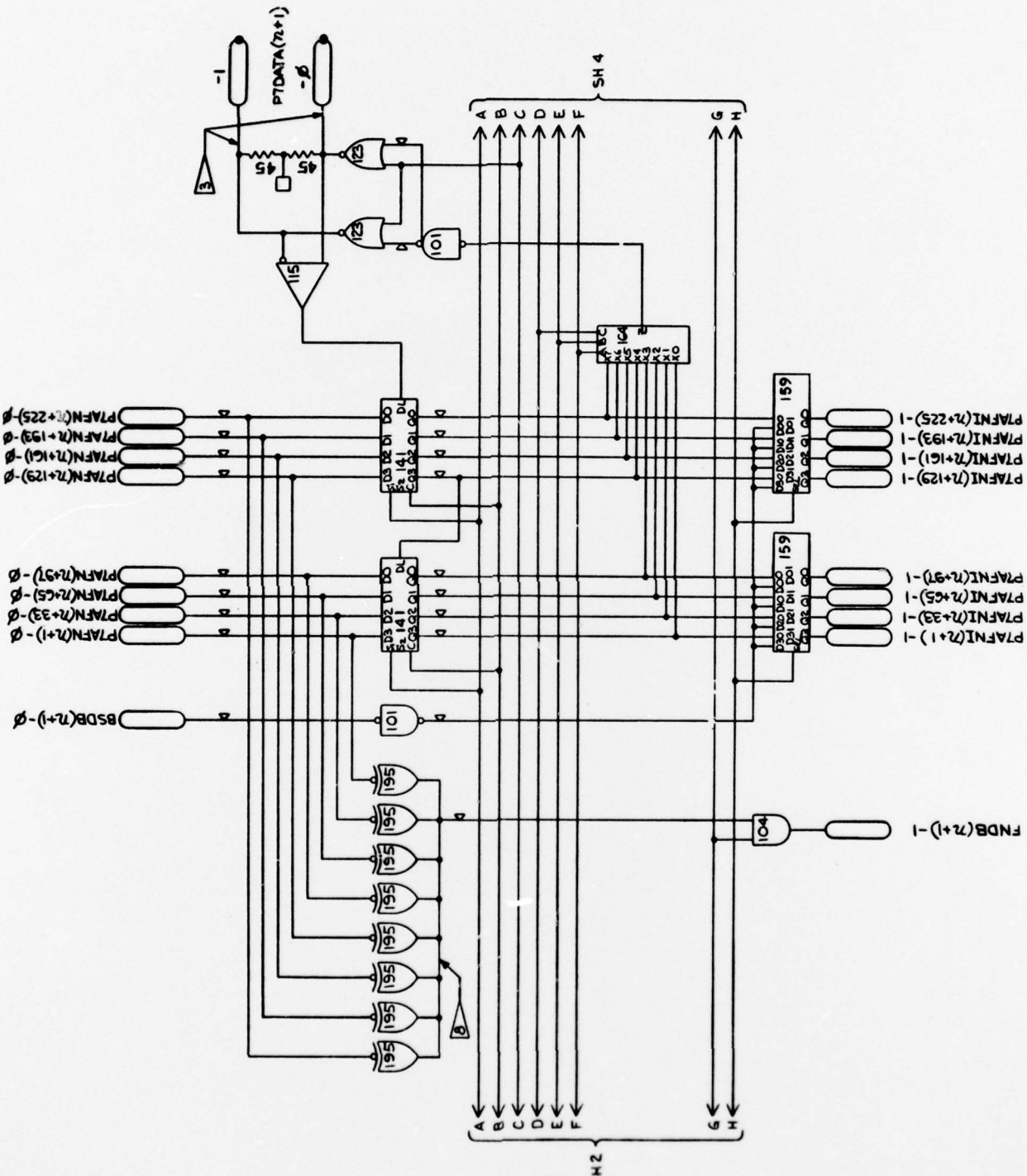


Figure A-2. PIO Port 7 Multiplexer PC Control Board (Sheet 3 of 5)

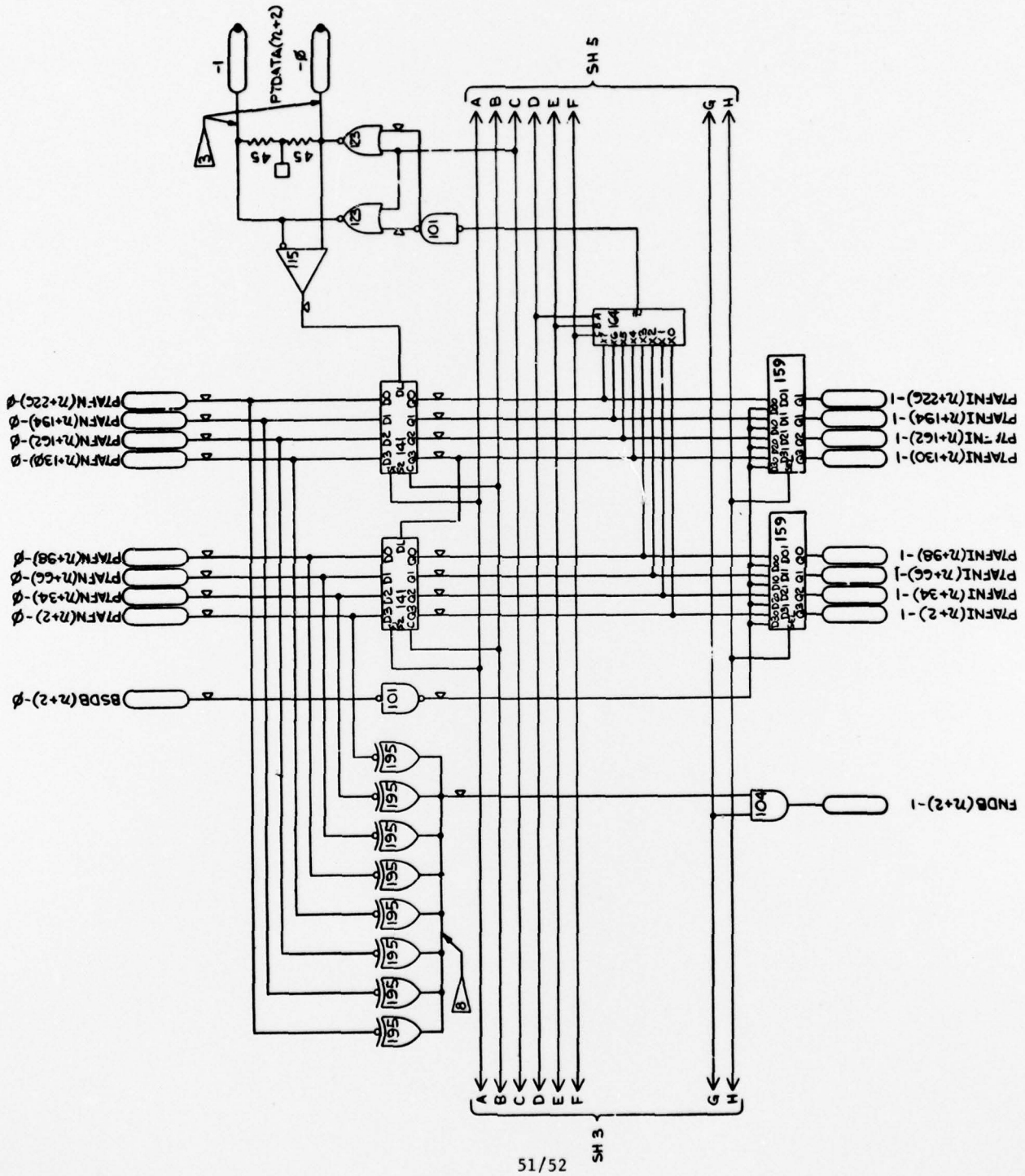


Figure A-2. PIO Port 7 Multiplexer PC Control Board (Sheet 4 of 5)

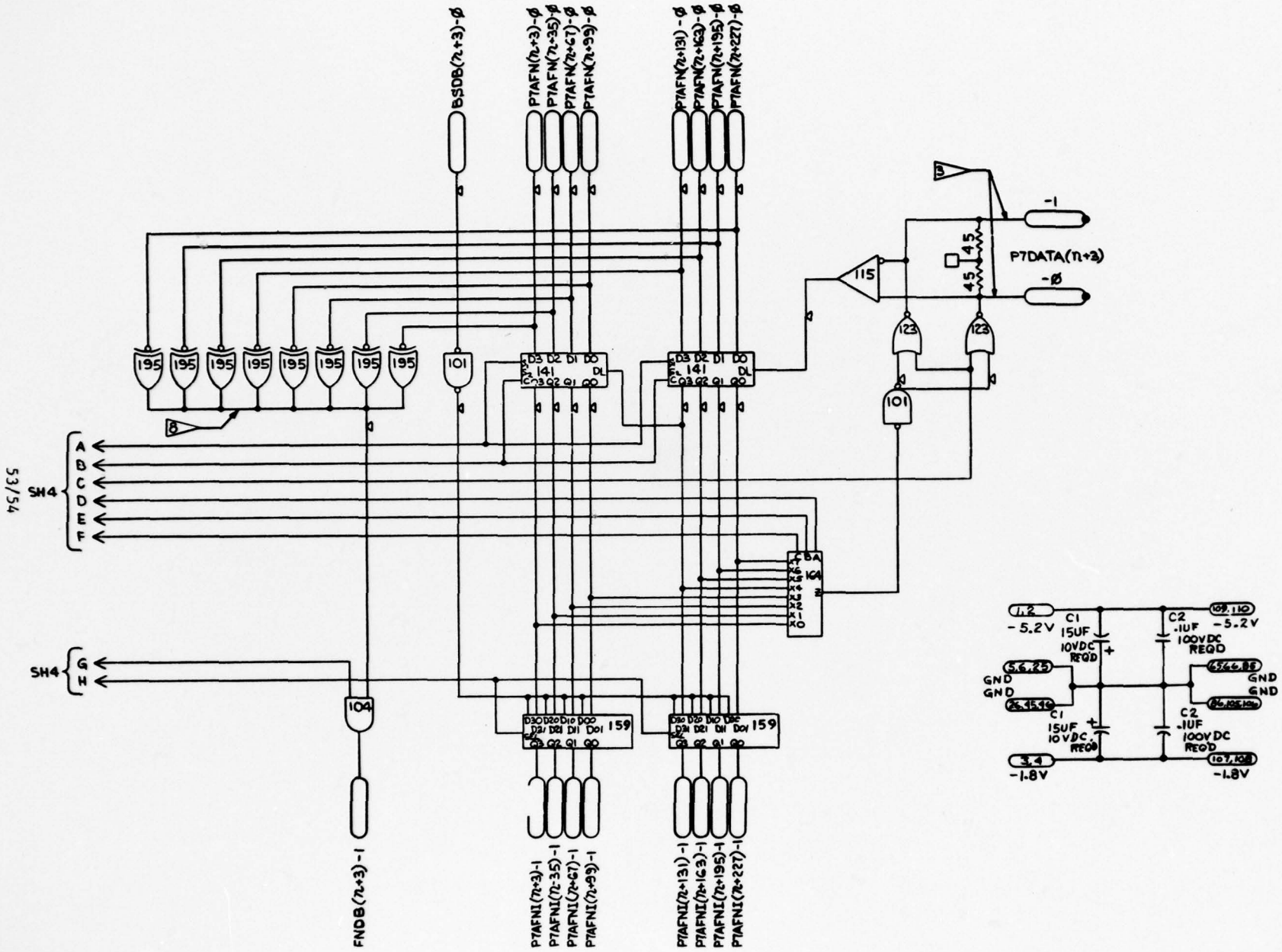
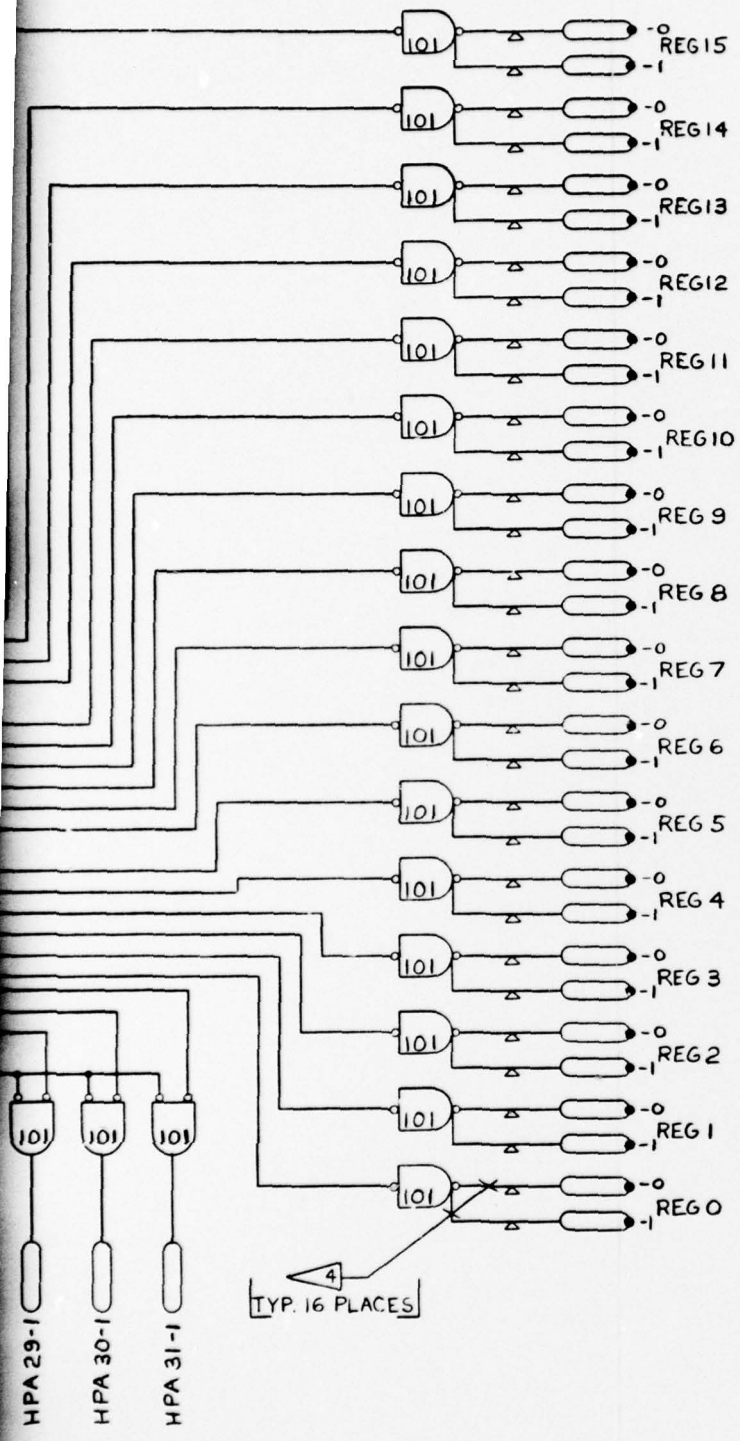


Figure A-2. PIO Port 7 Multiplexer PC Control Board (Sheet 5 of 5)

KHENIM-1
KHLDIM-1
510
510
101
101
DLHP 16-0
DLHP 17-0
DLHP 18-0
DLHP 19-0
DLHP 20-0
DLHP 21-0
DLHP 22-0
DLHP 23-0
DLHP 24-0
DLHP 25-0
DLHP 26-0
DLHP 27-0
DLHP 28-0
DLHP 29-0
DLHP 30-0
DLHP 31-0
-1
L
M
C 176
C 176
D1 D2 R2
C 131 Q1 Q2
D1 D2 R1 R2
C 131 Q1 Q2
HPA 16-1
HPA 17-1
HPA 18-1
HPA 19-1
HPA 20-1
HPA 21-1
HPA 22-1
HPA 23-1
HPA 24-1
HPA 25-1
HPA 26-1
HPA 27-1
HPA 28-1
HPA 29-1
HPA 30-1
HPA 31-1

Figu



NOTES:

1. OBSERVE WIRE-OR RULES
2. KEEP LINE LENGTH MINIMAL
3. FOIL LENGTH FROM GATE TO CONNECTOR ≤ 2 INCHES
4. DIFFERENTIAL PAIR. KEEP LINES PARALLEL AND MINIMAL LENGTH. USE CONNECTORS J1, J2, J3, J4 ONLY
5. LOGIC DIAGRAM SYMBOLS
   ⧈ = 91Ω, 1/8W RESISTOR TO -1.8V
   □ = -1.8VOLTS
   ◇ = -5.2VOLTS
6. I.C. NOS ARE PREFIXED BY "MC10" AND SUFFIXED BY "L"
7. NOS SHOWN ARE PAD NOS ON STD DIL. BD.
8. ALL RESISTORS ARE 91Ω, 1/8W

Figure A-3. PIO Port Expansion Control PC Board (Sheet 1 of 3) 55/56

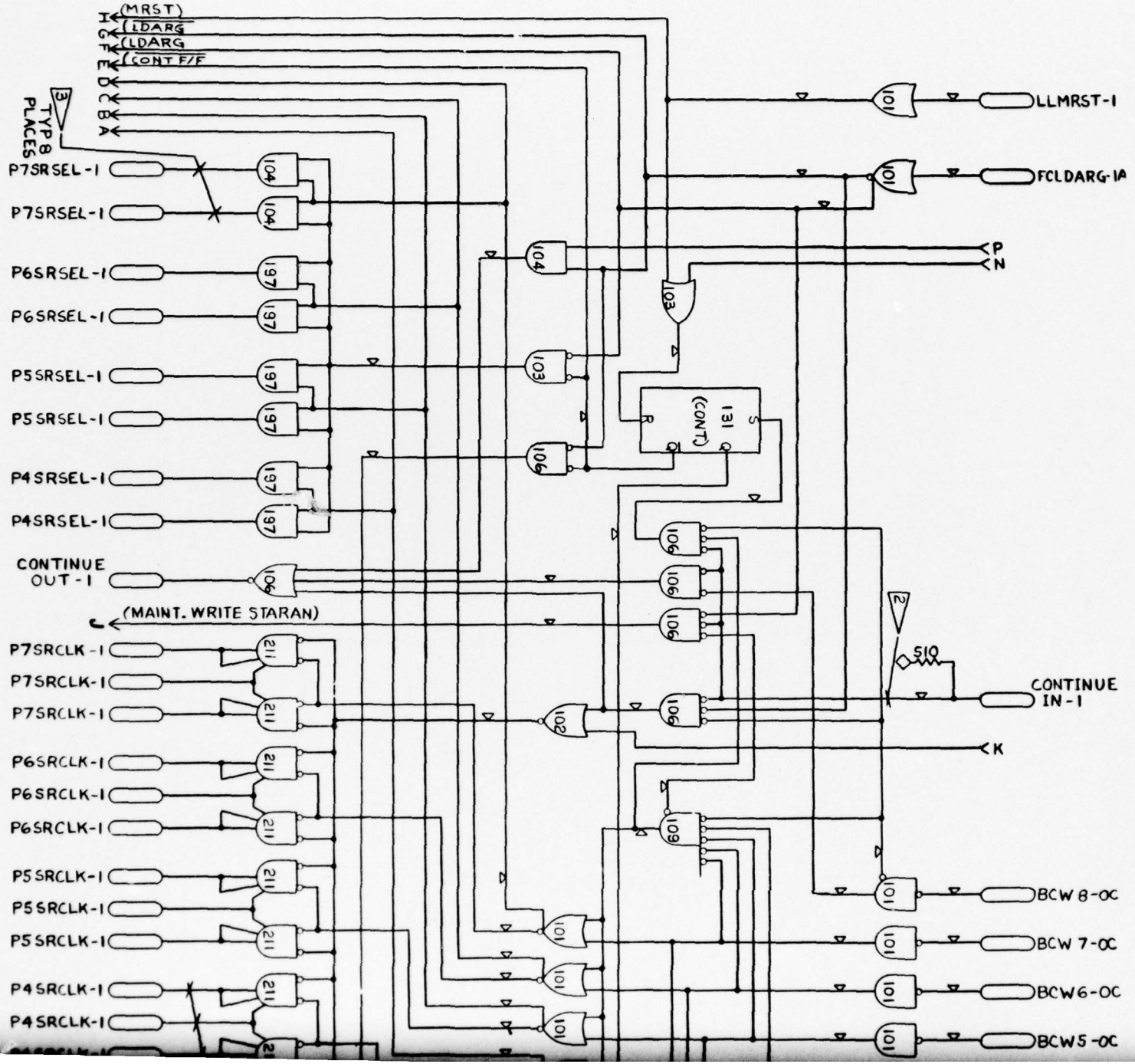

(MRST)
(LDARG
(LDARG
(CONT F/F
I
G
F
E
D
C
B
A
3 TYP 8 PLACES
P7SRSEL-1
P7SRSEL-1
P6SRSEL-1
P6SRSEL-1
P5SRSEL-1
P5SRSEL-1
P4SRSEL-1
P4SRSEL-1
CONTINUE OUT-1
(MAINT. WRITE STARAN)
P7SRCLK-1
P7SRCLK-1
P7SRCLK-1
P6SRCLK-1
P6SRCLK-1
P6SRCLK-1
P5SRCLK-1
P5SRCLK-1
P5SRCLK-1
P4SRCLK-1
P4SRCLK-1
LLMRST-1
FCLDARG-1A
P
N
131
S
R
(CONT)
2
510
CONTINUE IN-1
K
BCW 8-0C
BCW 7-0C
BCW6-0C
BCW5-0C

Figure A-3.

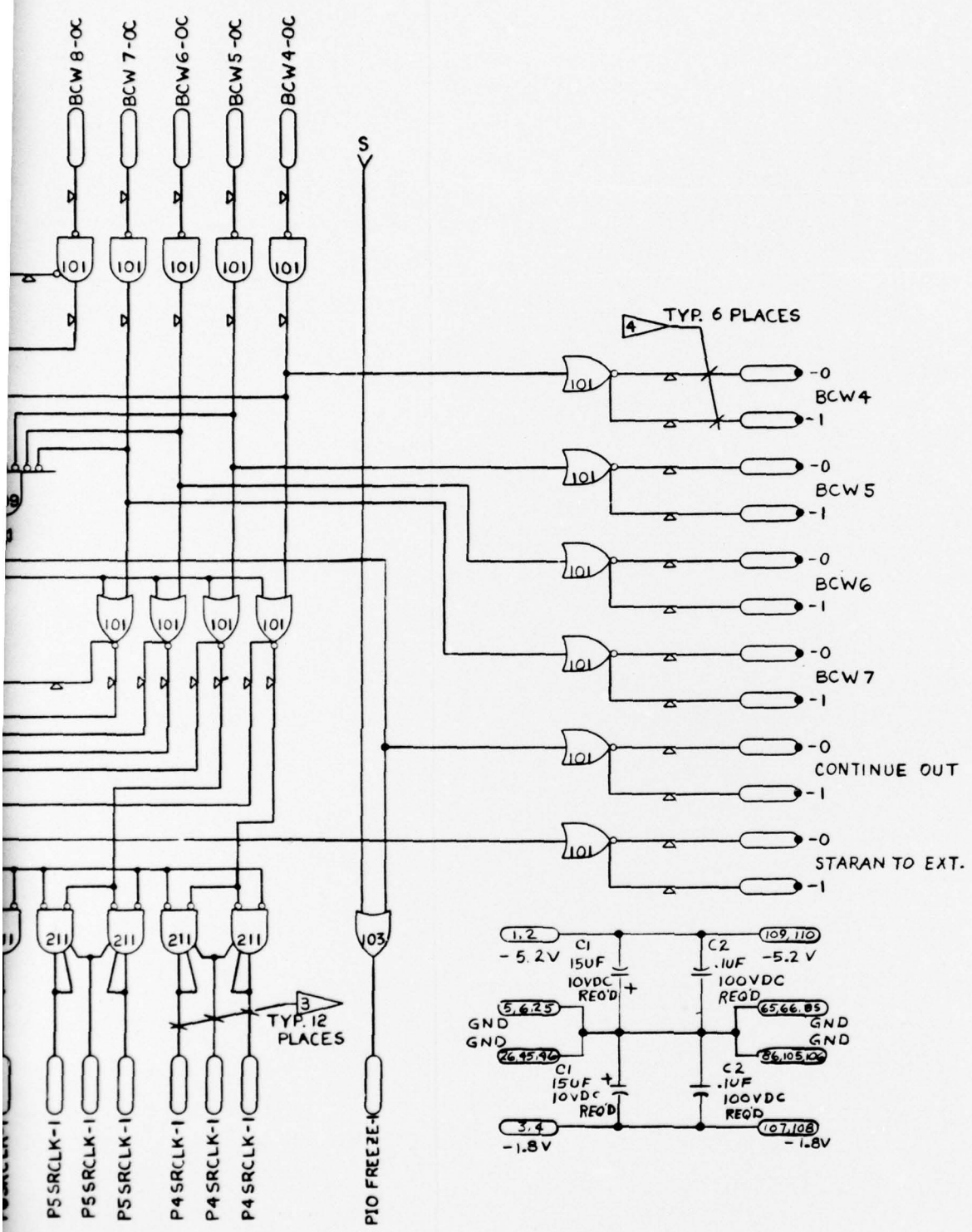


Figure A-3. PIO Port Expansion Control PC Board (Sheet 2 of 3) 57/58

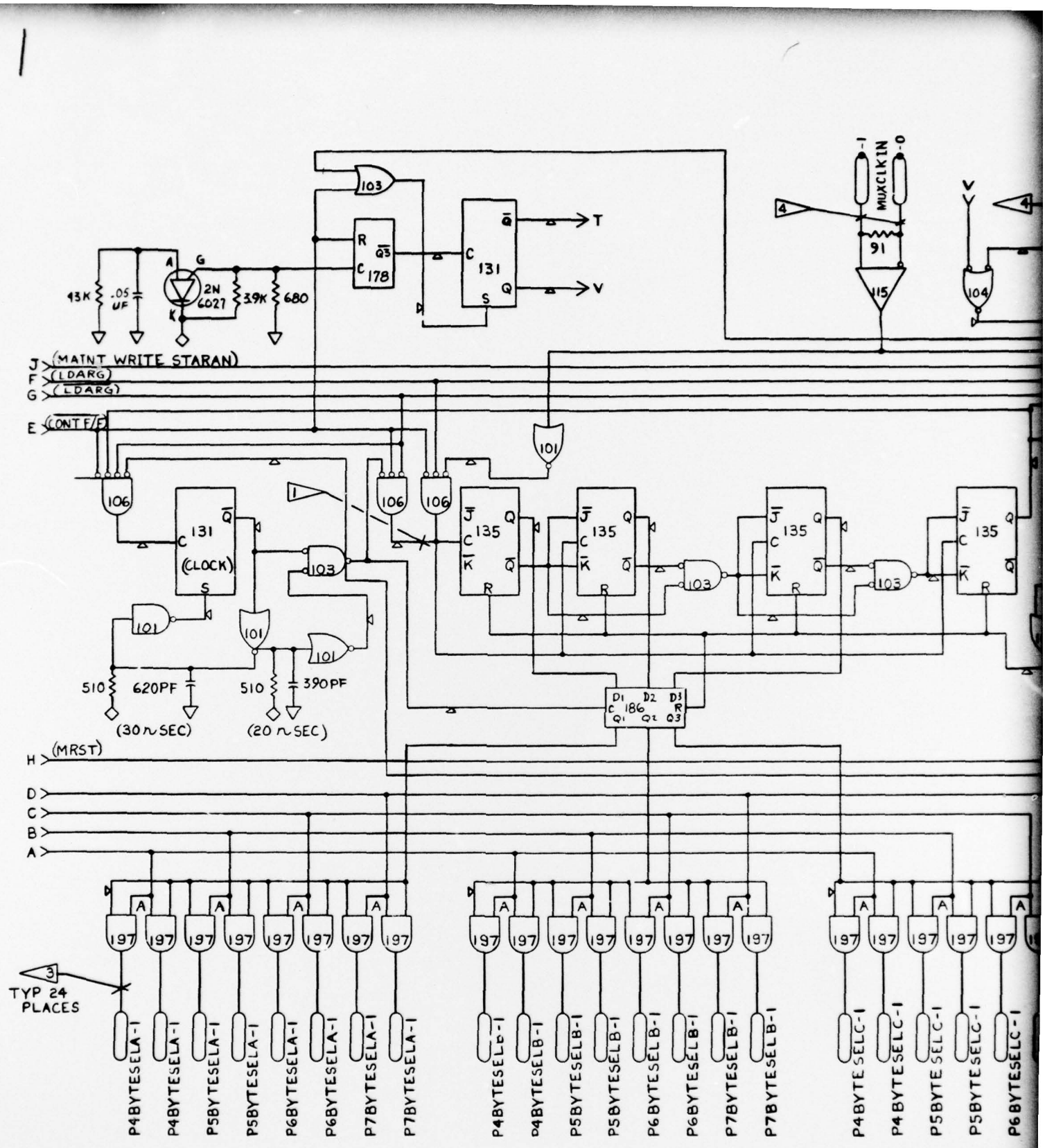


Figure A-3. PIO P

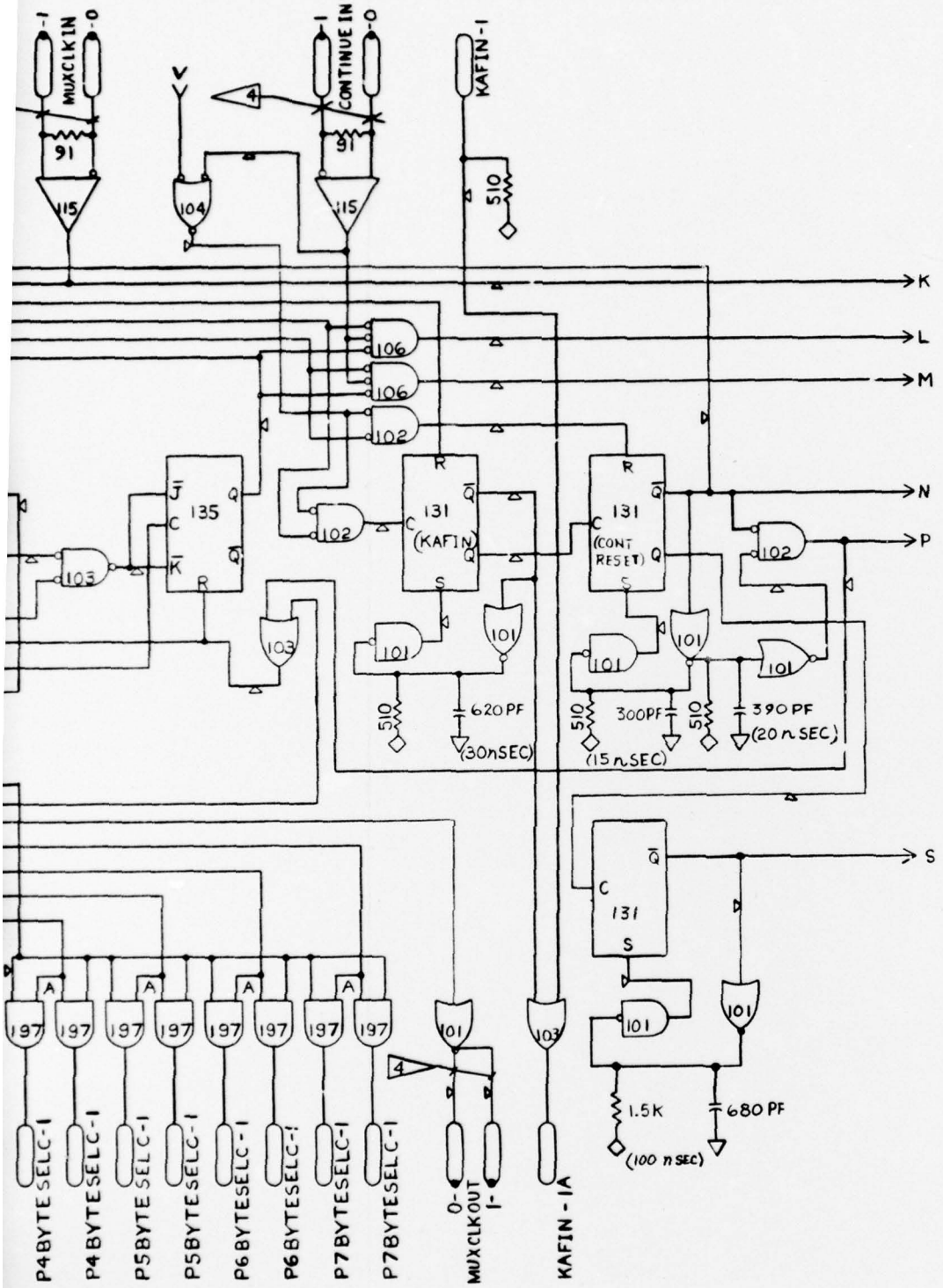


Figure A-3. PIO Port Expansion Control PC Board (Sheet 3 of 3) 59/60

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